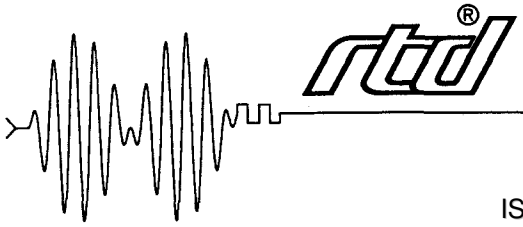
VF910 User's Manual



Real Time Devices, Inc.

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VF910

User's Manual

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INTRODUCTION

The VF910 variable resolution integrating analog I/O board turns your IBM PC/XT/AT or compatible computer into a high-performance data acquisition and control system. Installed within a single short or full-size expansion slot in the computer, the VF910 features:

- 8 differential, 8 single-ended with dedicated grounds, or 16 single-ended analog input channels,
- Resolution to 18 bits using a synchronous voltage-to-frequency converter,
- 0 to +5, 0 to +10, ±2.5, or ±5 volt input range,
- Programmable gains of 1, 2, 4, and 8 with an on-board gain multiplier circuit,
- Clock controlled A/D conversion,
- 16-bit sample counter,
- Software selectable system clock, interrupt source and interrupt channel,
- Trigger in and trigger out for external triggering or cascading boards,
- Two 12-bit analog output channels,
- ±5, ±10, 0 to +5, or 0 to +10 volt analog output range,
- Three user available 16-bit timer/counters,
- 16 8255-based TTL/CMOS compatible digital I/O lines,
- +5 volt operation.

The following paragraphs briefly describe the major functions of the board. More detailed discussions of board functions are included in Chapter 3, *Hardware Description*, and Chapter 4, *Board Operation and Programming*. The board setup is described in Chapter 1, *Board Settings*.

Analog-to-Digital Conversion

The analog-to-digital (A/D) conversion circuitry receives up to eight differential, eight single-ended with dedicated grounds, or 16 single-ended analog inputs and converts these inputs into frequencies. The frequencies are represented by 20-bit plus overflow words (in 3 x 8-bit format) which are read and/or transferred to PC memory.

An on-board header connector lets you jumper the inputs for differential or single-ended operation. When in the differential mode, the analog input channels can be individually set for single-ended or differential operation by configuring DIP switch S2. This feature lets you mix single-ended and differential input channels. Two unipolar and two bipolar ranges can be selected: 0 to +5, 0 to +10, ±2.5, or ±5 volts. The range is customer specified when ordering the board, and the board is calibrated for the selected range. Software programmable gains of 1, 2, 4, and 8 with an on-board gain multiplier circuitry let you customize the input range.

A/D conversions are performed by a voltage-to-frequency (V/F) converter. This exceptionally accurate converter technology lets you vary the resolution of your conversion while maintaining the full input voltage range. Instead, you trade speed for precision. For example, with a 1 MHz system clock and the input range set for 5 volts, 10-bit conversions are performed at a rate of 488 samples per seconds with a resolution of 4.88 millivolts, 12-bit conversions are performed at a rate of 122 samples per second with a resolution of 1.22 millivolts, and 18-bit conversions are performed at a rate of 2 samples per second with a resolution of 19 microvolts.

The converted data is read and/or transferred to PC memory, one byte at a time, through the PC data bus.

Digital-to-Analog Conversion

The digital-to-analog (D/A) circuitry features two independent 12-bit analog output channels with individually jumper-selectable output ranges of -5 to +5 volts, -10 to +10 volts, 0 to +5 volts, or 0 to +10 volts. Data is programmed into the D/A converter by writing two 8-bit words, the LSB and the MSB. Both outputs can be simultaneously updated by writing to an I/O port.

Digital I/O

The VF910 has 16 TTL/CMOS compatible digital I/O lines which can be directly interfaced with external devices or signals to sense switch closures, trigger digital events, or activate solid-state relays. These lines are provided by the 8255 programmable peripheral interface (PPI). Pads for installing and activating pull-up/pull-down resistors are included on the board. Installation procedures are given near the end of Chapter 1, *Board Settings*.

What Comes With Your Board

You receive the following items in your VF910 package:

- VF910 interface board
- Software and diagnostics diskette with example programs in BASIC, Pascal, and C source code
- rtdLinx TSR DOS driver
- User's manual

If any item is missing or damaged, please call Real Time Devices' Customer Service Department at (814) 234-8087. If you require service outside the U.S., contact your local distributor.

Board Accessories

In addition to the items included in your VF910 package, Real Time Devices offers a full line of software and hardware accessories. Call your local distributor or our main office for more information about these accessories and for help in choosing the best items to support your board's application.

Application Software and Drivers

Our custom application software packages provide excellent data acquisition and analysis support. Use SIGNAL*VIEW for monitoring and data acquisition, or SIGNAL*MATH for integrated data acquisition and sophisticated digital signal processing and analysis. rtdLinx (included with your board) and rtdLinx/NB drivers provide full-featured high level interfaces between the board and custom or third party software, including Labtech Notebook, Notebook/XE, and LT/Control. rtdLinx source code is available for a one-time fee.

Hardware Accessories

Hardware accessories for the VF910 include the TMX32 analog input expansion board with thermocouple compensation which can expand a single input channel on your board to 16 differential or 32 single-ended input channels, MR series mechanical relay output boards, OP series optoisolated digital input boards, the OR16 mechanical relay/optoisolated digital I/O board, the USF8 universal sensor front-end with sensor excitation, the TB50 terminal board and XB50 prototype/terminal board for prototype development and easy signal access, the EX-XT extender board for simplified testing and debugging of prototype circuitry, and the XT50 twisted pair ribbon cable assembly for external interfacing.

Using This Manual

This manual is intended to help you install your new board and get it running quickly, while also providing enough detail about the board and its functions so that you can enjoy maximum use of its features even in the most complex applications. We assume that you already have an understanding of data acquisition principles and that you can customize the example software or write your own applications programs.

When You Need Help

This manual and the example programs in the software package included with your board provide enough information to properly use all of the board's features. If you have any problems installing or using this board, contact our Technical Support Department, (814) 234-8087, during regular business hours, eastern standard time or eastern daylight time, or send a FAX requesting assistance to (814) 234-5218. When sending a FAX request, please include your company's name and address, your name, your telephone number, and a brief description of the problem.

CHAPTER 1

BOARD SETTINGS

The VF910 board has jumper and switch settings you can change if necessary for your application. The board is factory-configured as listed in the table and shown on a diagram in the beginning of this chapter. Should you need to change these settings, use these easy-to-follow instructions before you install the board in your computer.

Note that by installing resistor packs at three locations around the 8255 PPI and soldering jumpers in the associated pads, you can configure the 16 available digital I/O lines to be pulled up or pulled down. This procedure is explained near the end of this chapter.

Also note that by installing resistive components, you can add your own gain multiplier for the software programmable binary gains of 1, 2, 4, and 8. The gain multiplier circuitry is described at the end of this chapter.

Factory-Configured Switch and Jumper Settings

Table 1-1 lists the factory settings of the user-configurable switch and jumpers on the VF910 board. Figure 1-1 shows the board layout and the locations of the factory-set jumpers. The following paragraphs explain how to change the factory settings.

Table 1-1 — Factory Settings

Switch/ Jumper	Function Controlled	Factory Setting
P3	Sets the user timer/counter output signals available at P2-43 and P2-44	P2-43: TRIG, P2-44: OUT0
P4	Sets the clock sources for the user timer/counters	CLK0: OSC, CLK1: OT0, CLK2: OT1 (cascaded)
P5	Sets the gate sources for the user timer/counters	GATE0: +5V, GATE1: +5V, GATE2: +5V
P6	Sets the analog inputs as 16 single-ended or 8 single-ended with GND/8 differential; used with S2	16 single-ended (3 jumpers installed on S pins)
P7	Sets the analog input voltage range and polarity	5V, BI (-2.5 to +2.5 volts)
P8	Sets the D/A output voltage range for DAC 1	±5, X1 (-5 to +5 volts)
P9	Sets the D/A output voltage range for DAC 2	±5, X1 (-5 to +5 volts)
S1	Sets the base address	300 hex (768 decimal)
S2	Connects the negative side of differential inputs to ground for 8 single-ended with ground operation	OPEN (16 single-ended)

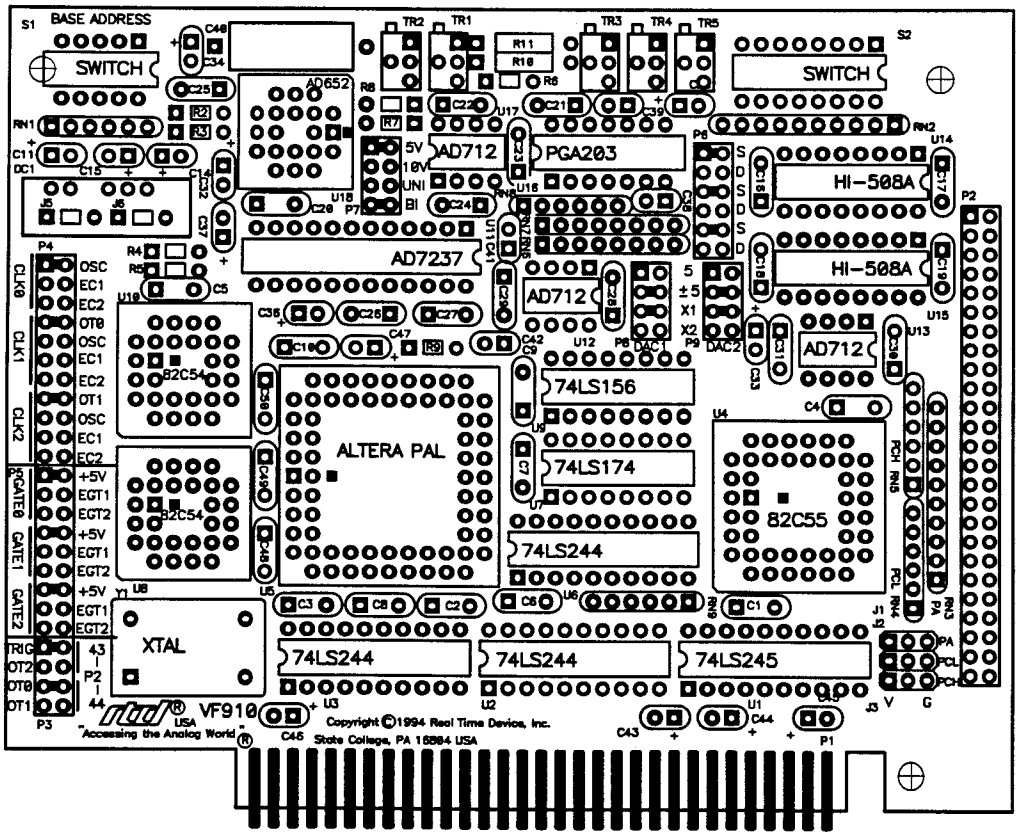


Fig. 1-1 — Board Layout Showing Factory-Configured Settings

P3 — User Timer/Counter Output Select (Factory Setting: P2-43: TRIG, P2-44: OT0)

This header connector, shown in Figure 1-2, lets you select one of two signals to be present at each of two of the P2 I/O connector pins, P2-43 and P2-44. This allows you more flexibility when setting up the board. P2-43 can be configured to provide an external trigger (TRIG) or the output of user timer/counter 2 (OT2). P2-44 can be configured to provide the output of user timer/counter 0 (OT0) or the output of user timer/counter 1 (OT1). Note that when you cascade multiple boards, you must configure P2-43 to carry the external trigger signal (TRIG) on each board that outputs a trigger to the next board in the chain.

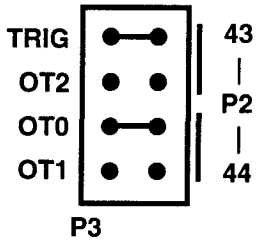


Fig. 1-2 — User Timer/Counter Output Select Jumpers, P3

P4 — User Timer/Counter Clock Source (Factory Settings: CLK0-OSC, CLK1-OT0, CLK2-OT1)

This header connector, shown in Figure 1-3, lets you select the clock sources for the user available 8254 timer/counters, TC0, TC1, and TC2. The factory setting cascades all three timer/counters, with the clock source for TC0 being the on-board 2 MHz oscillator, the output of TC0 providing the clock for TC1, and the output of TC1 providing the clock for TC2. You can connect any or all of the sources to either of two external clock inputs (the first source labeled EC1 on the header and EXT CLK1 at P2-41, and the second source labeled EC2 on the header and EXT CLK2 at P2-45), or you can set TC1 and TC2 to be clocked by the 2 MHz oscillator. Figure 1-4 shows a block diagram of the timer/counter circuitry to help you with these connections.

NOTE: When installing jumpers on this header, make sure that only one jumper is installed in each group of three or four CLK pins.

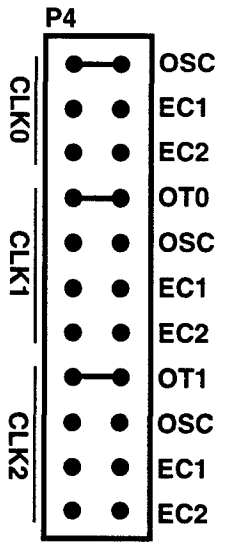


Fig. 1-3 — User Timer/Counter Clock Source Jumpers, P4

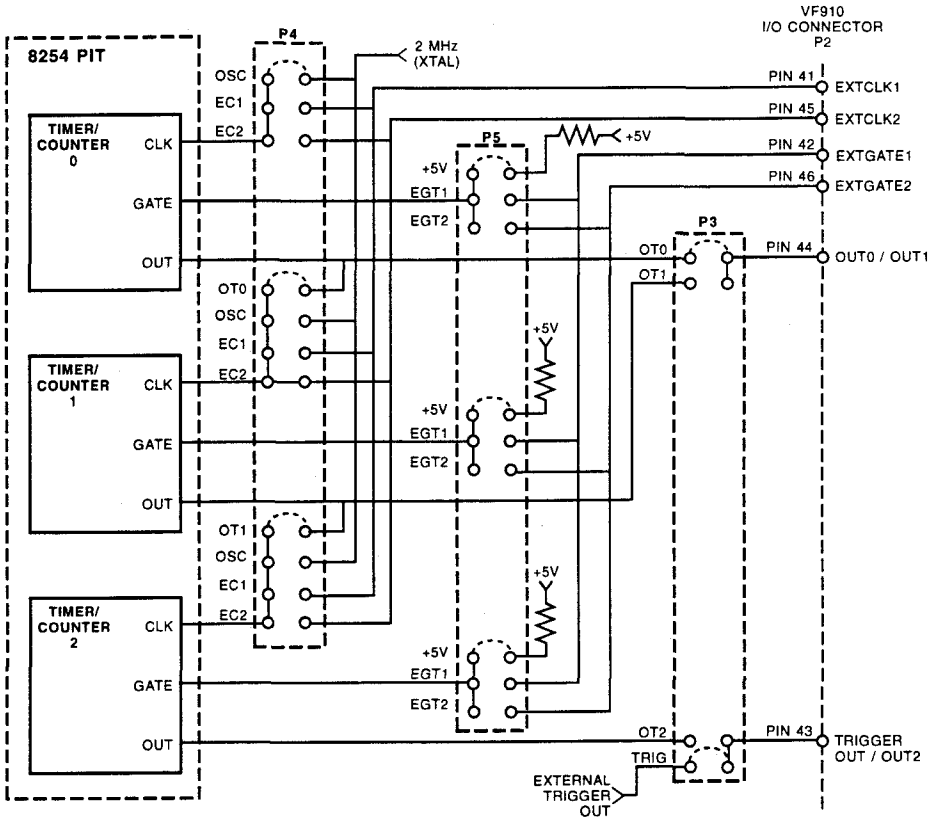


Fig. 1-4 — 8254 Timer/Counter Circuit Block Diagram

P5 — User Timer/Counter Gate Source (Factory Settings: All Gates: +5V)

This header connector, shown in Figure 1-5, lets you select the gate sources for the user available 8254 timer/counters, TC0, TC1, and TC2. The factory setting ties all three gates high, to an on-board +5 volt source. You can connect any or all of the gates to either of two external gate inputs (the first source labeled EGT1 on the header and EXT GATE1 at P2-42, and the second source labeled EGT2 on the header and EXT GATE2 at P2-46). Figure 1-4 shows a block diagram of the timer/counter circuitry to help you with these connections.

NOTE: When installing jumpers on this header, make sure that only one jumper is installed in each group of three GATE pins.

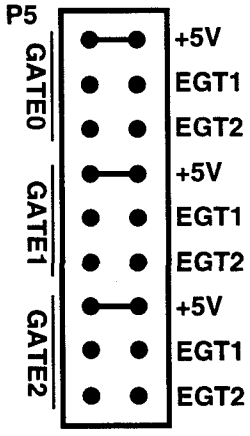


Fig. 1-5 — User Timer/Counter Gate Source Jumpers, P5

P6 — Single-Ended/Differential Analog Inputs (Factory Setting: S (16 Single-Ended))

This header connector, shown in Figure 1-6, is used with switch S2 to configure the VF910 for 8 differential, 8 single-ended with dedicated grounds, or 16 single-ended analog input channels. When operating in the 16 input single-ended mode, three jumpers must be installed across the S pins. When operating in the 8 single-ended with dedicated grounds or 8 differential mode, three jumpers must be installed across the D pins. The switch settings on S2 can then be used to individually configure channels for single-ended or differential operation. DO NOT install jumpers across both S and D pins at the same time!

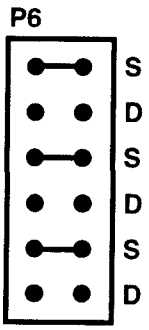


Fig. 1-6 — Single-Ended/Differential Analog Input Signal Type Jumpers, P6

P7 — Analog Input Voltage Range and Polarity (Factory Setting: 5V, BI (±2.5 Volts))

P7, shown in Figure 1-7, sets the analog input voltage range and polarity. The board can be set up to operate over a range of 5 or 10 volts, unipolar or bipolar. The board's four possible ranges are 0 to +5, 0 to +10, ±2.5, and ±5 volts. The range and polarity are set according to your specifications when ordering the board. Figure 1-7 shows the factory setting of -2.5 to +2.5 volts (if no range was specified when ordering).

NOTE: If you change the analog input range and/or polarity, you should recalibrate the board according to the instructions in Chapter 6, *Calibration.* Otherwise, you may get erroneous data.

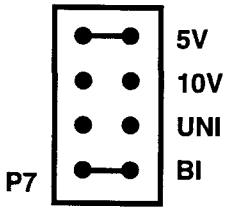


Fig. 1-7 — Analog Input Voltage Range and Polarity, P7

P8 — DAC 1 Output Voltage Range (Factory Setting: +5 to -5 volts)

This header connector, shown in Figure 1-8, sets the output voltage range for DAC 1 at 0 to +5, ±5, 0 to +10, or ±10 volts. Two jumpers must be installed, one to select the range and one to select the multiplier. The top two jumpers select the range, bipolar (±5) or unipolar (5). The bottom two jumpers select the multiplier, X2 or X1. When a jumper is on the X2 multiplier pins, the range values become ±10 and 10. The table on the next page shows the four possible combinations of jumper settings. This header does not have to be set the same as P9.

Voltage Range	Jumpers (Top to Bottom)			
	5	±5	X1	X2
-5 to +5 volts	OFF	ON	ON	OFF
0 to +5 volts	ON	OFF	ON	OFF
-10 to +10 volts	OFF	ON	OFF	ON
0 to +10 volts	ON	OFF	OFF	ON

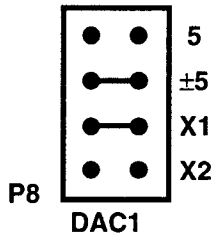


Fig. 1-8 — DAC 1 Output Voltage Range Jumper, P8

P9 — DAC 2 Output Voltage Range (Factory Setting: +5 to -5 volts)

This header connector, shown in Figure 1-9, sets the output voltage range for DAC 2 at 0 to +5, ±5, 0 to +10, or ±10 volts. Two jumpers must be installed, one to select the range and one to select the multiplier. The top two jumpers select the range, bipolar (±5) or unipolar (5). The bottom two jumpers select the multiplier, X2 or X1. When a jumper is on the X2 multiplier pins, the range values become ±10 and 10. The table below shows the four possible combinations of jumper settings. This header does not have to be set the same as P8.

Voltage Range	Jumpers (Top to Bottom)			
	5	±5	X1	X2
-5 to +5 volts	OFF	ON	ON	OFF
0 to +5 volts	ON	OFF	ON	OFF
-10 to +10 volts	OFF	ON	OFF	ON
0 to +10 volts	ON	OFF	OFF	ON

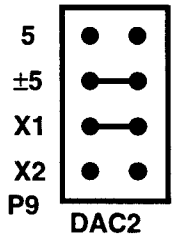


Fig. 1-9 — DAC 2 Output Voltage Range Jumper, P9

S1 — Base Address (Factory Setting: 300 hex (768 decimal))

One of the most common causes of failure when you are first trying your board is address contention. Some of your computer's I/O space is already occupied by internal I/O and other peripherals. When the board attempts to use I/O address locations already used by another device, contention results and the board does not work.

To avoid this problem, the VF910 has an easily accessible five-position DIP switch, S1, which lets you select any one of 16 starting addresses in the computer's I/O. Should the factory setting of 300 hex (768 decimal) be unsuitable for your system, you can select a different base address simply by setting the switches to any one of the values listed in Table 1-2. The table shows the switch settings and their corresponding decimal and hexadecimal (in parentheses) values. Make sure that you verify the order of the switch numbers on the switch (1 through 4) before setting them. When the switches are pulled forward, they are OPEN, or set to logic 1, as labeled on the DIP switch package. When you set the base address for your board, record the value in the table inside the back cover. Figure 1-10 shows the DIP switch set for a base address of 300 hex (768 decimal).

Table 1-2 — Base Address Switch Settings, S1

Base Address Decimal / (Hex)	Switch Setting 4 3 2 1	Base Address Decimal / (Hex)	Switch Setting 4 3 2 1
512 / (200)	0 0 0 0	768 / (300)	1 0 0 0
544 / (220)	0 0 0 1	800 / (320)	1 0 0 1
576 / (240)	0 0 1 0	832 / (340)	1 0 1 0
608 / (260)	0 0 1 1	864 / (360)	1 0 1 1
640 / (280)	0 1 0 0	896 / (380)	1 1 0 0
672 / (2A0)	0 1 0 1	928 / (3A0)	1 1 0 1
704 / (2C0)	0 1 1 0	960 / (3C0)	1 1 1 0
736 / (2E0)	0 1 1 1	992 / (3E0)	1 1 1 1
0 = closed, 1 = open			

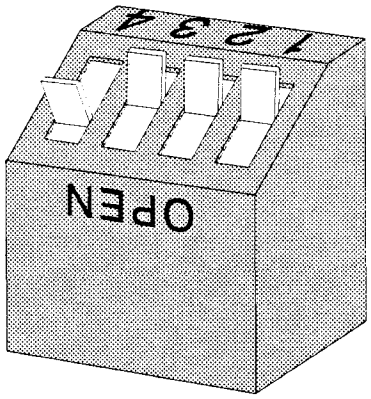
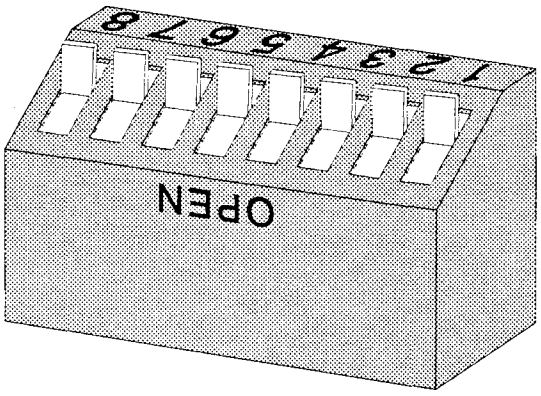


Fig. 1-10 — Base Address Switch, S1

S2 — Differential/Single-Ended Ground Switch (Factory Setting: OPEN)

DIP switch S2, shown in Figure 1-11, is used in conjunction with header connector P6 to set up the analog inputs for 8 differential, 8 single-ended with dedicated grounds, or 16 single-ended operation. When the eight switches are OPEN (forward), they support 8 differential or 16 single-ended inputs, depending on the setting of P6. When the switches are CLOSED (back), they support 8 single-ended inputs with dedicated grounds. With P6 set to D, switches can be individually set for differential or single-ended with ground operation. Switch 1 sets channel 1, switch 2 sets channel 2, etc. The table below shows the three configurations for P6 and S2.



Input Configuration	Settings	
	P6 Jumpers	S2 Switches
8 DIFF	D	OPEN
8 SE with AGND	D	CLOSED
16 SE	S	OPEN

Fig. 1-11 — Differential/Single-Ended Ground Switch, S2

Pull-up/Pull-down Resistors on Digital I/O Lines

The 8255 programmable peripheral interface provides 16 TTL/CMOS compatible digital I/O lines which can be interfaced with external devices. These lines are divided into three groups: eight Port A lines, four Port C Lower lines, and four Port C Upper lines. (The eight lines of Port B are used for internal board functions.) You can install and connect pull-up or pull-down resistors for any or all of these three groups of lines. You may want to pull lines up for connection to switches. This will pull the line high when the switch is disconnected. Or, you may want to pull lines down for connection to relays which control turning motors on and off. These motors turn on when the digital lines controlling them are high. The Port A lines of the 8255 automatically power up as inputs, which can float high during the few moments before the board is first initialized. This can cause the external devices connected to these lines to operate erratically. By pulling these lines down, when the data acquisition system is first turned on, the motors will not switch on before the 8255 is initialized.

To use the pull-up/pull-down feature, you must first install resistor packs in any or all of the three locations between the 8255 and I/O connector, labeled PA, PCL, and PCH. PA takes a 10-pin pack, and PCL and PCH take 6-pin packs.

After the resistor packs are installed, you must connect them into the circuit as pull-ups or pull-downs. Locate the three-hole pads on the board below the resistor packs. They are labeled G (for ground) on one end and V (for +5V) on the other end. The middle hole is common. PA is for Port A, PCL is for Port C Lower, and PCH is for Port C Upper. To operate as pull-ups, solder a jumper wire between the common pin (middle pin of the three) and the V pin. For pull-downs, solder a jumper wire between the common pin (middle pin) and the G pin. Figure 1-12 shows Port A lines with pull-ups, Port C Lower with pull-downs, and Port C Upper with no resistors.

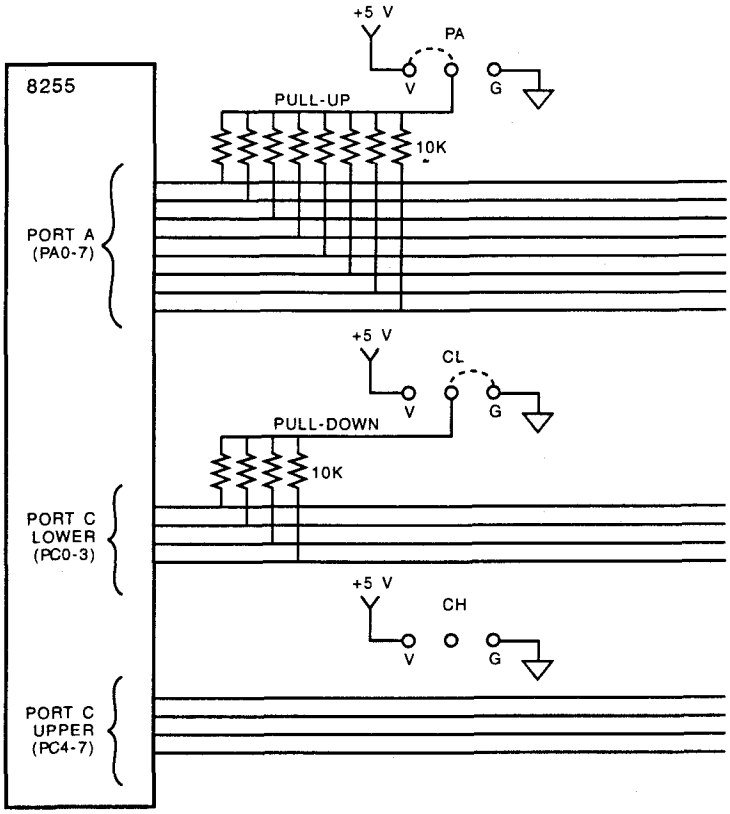


Fig. 1-12 — Adding Pull-ups and Pull-downs to Digital I/O Lines

Gm, Gain Multiplier Circuitry

The VF910 has software programmable binary gains of 1, 2, 4, and 8. A gain multiplier circuit, Gm, is provided so that you can easily configure special gain settings for a specific application. Note that when you use this feature and set up the board for a gain of other than 1, all of the input channels will operate only at your custom gain settings. In other words, if you install circuitry which gives you a gain multiplier of 10, then the four programmable gains available are 10, 20, 40, and 80.

Gm is derived by adding resistors R10 and R11 and trimpot TR3, all located in the upper center area of the board. The resistors and trimpot combine to set the gain, as shown in the diagram and formula in Figure 1-13.

As shown in Figure 1-13, a solder short must be removed from the board to activate the Gm circuitry. This short is located on the **bottom side** of the board under U17 (AD712 IC). Figure 1-14 shows the location of the solder short.

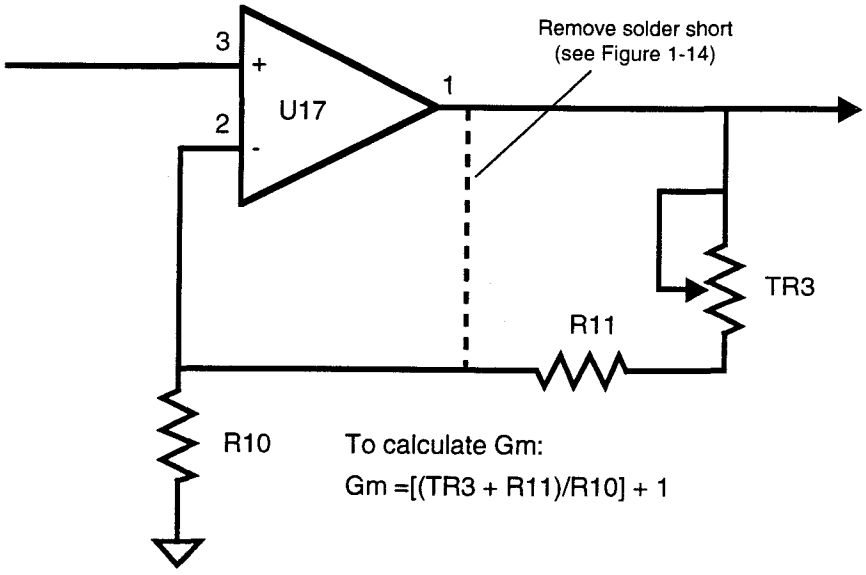


Fig. 1-13 — Gain Circuitry and Formula for Calculating Gm

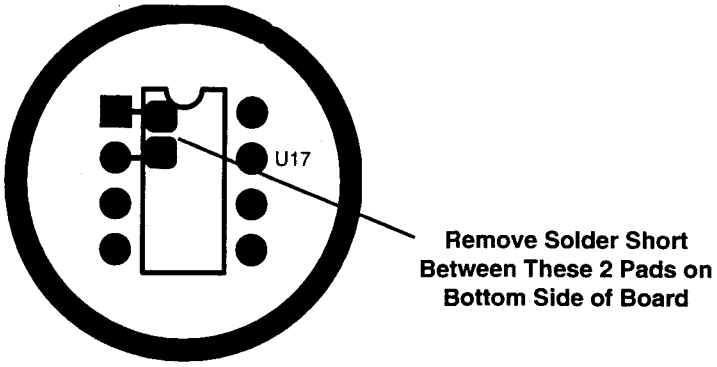


Fig. 1-14 — Diagram for Removal of Solder Short

CHAPTER 2

BOARD INSTALLATION

The VF910 board is easy to install in your IBM PC/XT/AT or compatible computer. It can be placed in any slot, short or full-size. This chapter tells you step-by-step how to install and connect the board.

Board Installation

Keep the board in its antistatic bag until you are ready to install it in your computer. When removing it from the bag, hold the board at the edges and do not touch the components or connectors.

Before installing the board in your computer, check the jumper settings. Chapter 1 reviews the factory settings and how to change them. If you need to change any settings, refer to the appropriate instructions in Chapter 1. Note that incompatible jumper settings can result in unpredictable board operation and erratic response.

To install the board:

1. Turn OFF the power to your computer.
2. Remove the top cover of the computer housing (refer to your owner's manual if you do not already know how to do this).
4. Select any unused short or full-size expansion slot and remove the slot bracket.
5. Touch the metal housing of the computer to discharge any static buildup and then remove the board from its antistatic bag.
6. Holding the board by its edges, orient it so that its card edge (bus) connector lines up with the expansion slot connector in the bottom of the selected expansion slot.
7. After carefully positioning the board in the expansion slot so that the card edge connector is resting on the computer's bus connector, gently and evenly press down on the board until it is secured in the slot.

   NOTE: Do not force the board into the slot. If the board does not slide into place, remove it and try again. Wiggling the board or exerting too much pressure can result in damage to the board or to the computer.
8. After the board is installed, secure the slot bracket back into place and put the cover back on your computer. The board is now ready to be connected via the external I/O connector at the rear panel of your computer.

External I/O Connections

Figure 2-1 shows the VF910's P2 I/O connector pinout. Refer to this diagram as you make your I/O connections.

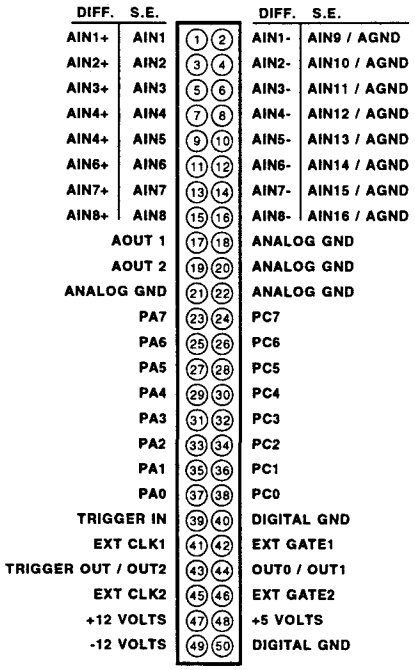

DIFF. S.E.
AIN1+ AIN1 1 2 AIN1- AIN9 / AGND
AIN2+ AIN2 3 4 AIN2- AIN10 / AGND
AIN3+ AIN3 5 6 AIN3- AIN11 / AGND
AIN4+ AIN4 7 8 AIN4- AIN12 / AGND
AIN4+ AIN5 9 10 AIN5- AIN13 / AGND
AIN6+ AIN6 11 12 AIN6- AIN14 / AGND
AIN7+ AIN7 13 14 AIN7- AIN15 / AGND
AIN8+ AIN8 15 16 AIN8- AIN16 / AGND
AOUT 1 17 18 ANALOG GND
AOUT 2 19 20 ANALOG GND
ANALOG GND 21 22 ANALOG GND
PA7 23 24 PC7
PA6 25 26 PC6
PA5 27 28 PC5
PA4 29 30 PC4
PA3 31 32 PC3
PA2 33 34 PC2
PA1 35 36 PC1
PA0 37 38 PC0
TRIGGER IN 39 40 DIGITAL GND
EXT CLK1 41 42 EXT GATE1
TRIGGER OUT / OUT2 43 44 OUT0 / OUT1
EXT CLK2 45 46 EXT GATE2
+12 VOLTS 47 48 +5 VOLTS
-12 VOLTS 49 50 DIGITAL GND

Fig. 2-1 — P2 I/O Connector Pin Assignments

Connecting the Analog Input Pins

16 Single-Ended, No Dedicated GND. When operating in the 16 channel single-ended mode (P6-S, S2-OPEN), connect the high side of the analog inputs to the analog input channels, AIN1 through AIN16, and connect the low side to any of the ANALOG GND pins available at the connector (pins 18, 20-22 on P2). Ground any unused inputs. Figure 2-2 shows how these connections are made.

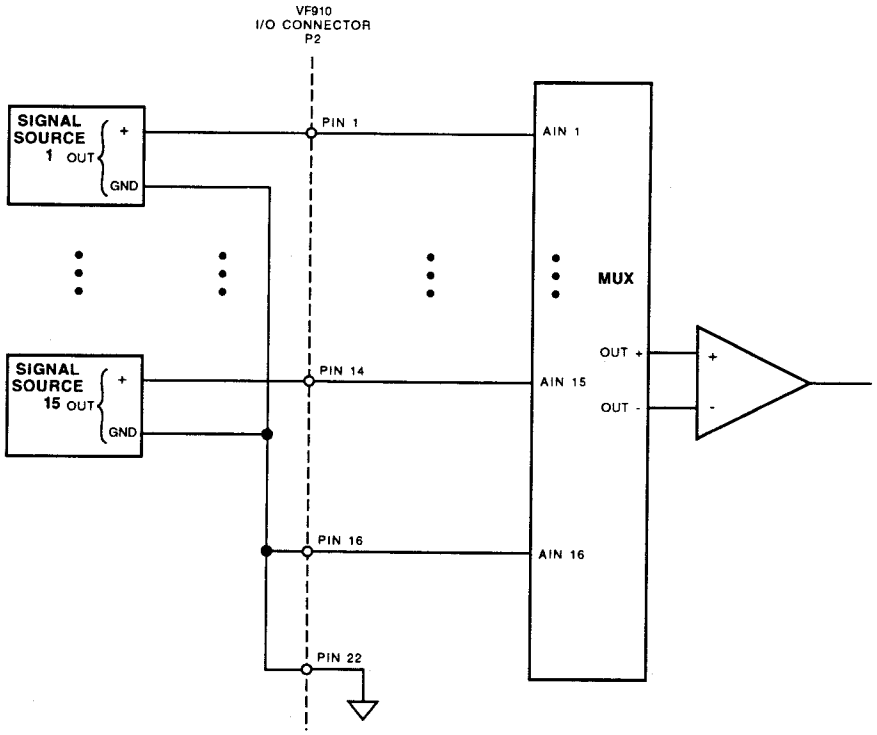


Fig. 2-2 — Single-Ended Input Connections

8 Single-Ended, Dedicated GND. When operating up to 8 channels in the single-ended mode with a dedicated ground for each channel (P6-D, S2-CLOSED), connect the high side of each analog input to the selected analog input channel, AIN1 through AIN8, and connect the low side to its corresponding AGND (AIN1- through AIN8-). Ground any unused inputs. Figure 2-3 shows how these connections are made. Note that you can mix single-ended with dedicated ground and differential channels by setting the individual switches on S2 to the proper position.

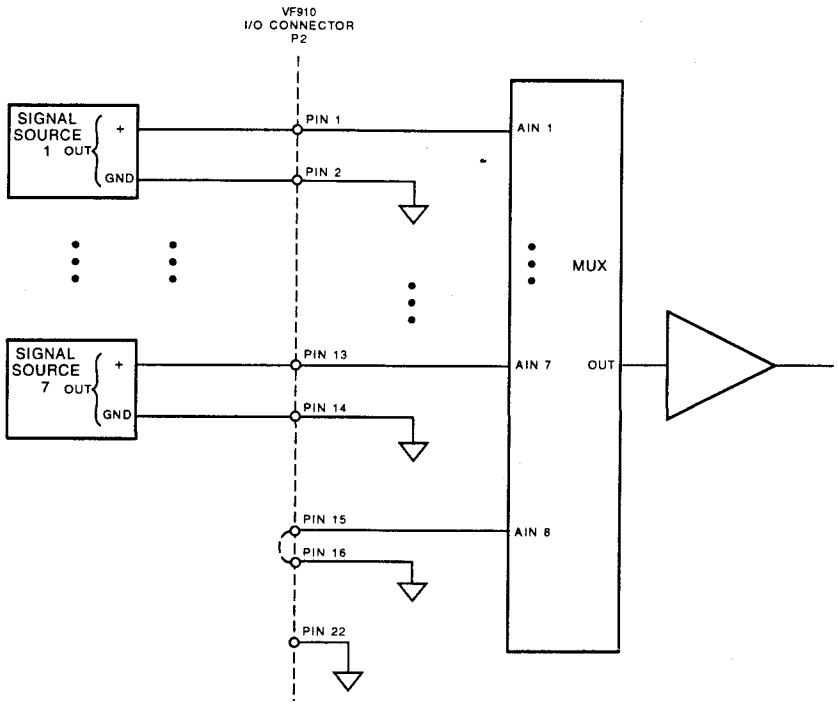


Fig. 2-3 — Single-Ended with Dedicated Grounds Input Connections

8 Differential. When operating in the differential mode (P6-D, S2-OPEN), twisted pair cable is recommended to reduce the effects of magnetic coupling at the input. Your signal source may or may not have a separate ground reference. When using the differential mode, you should install a 10 kilohm resistor pack at RN2 on the board to provide a reference to ground for signal sources without a separate ground reference.

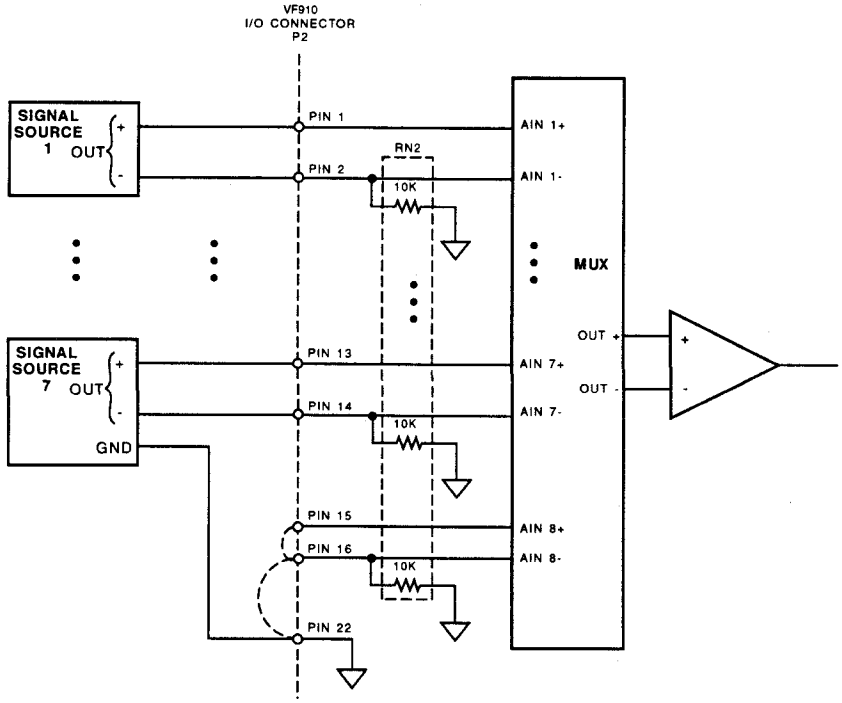


Fig. 2-4 — Differential Input Connections

Connect the high side of the analog input to the selected analog input channel, AIN1+ through AIN8+, and connect the low side to the corresponding AIN- pin. Then, for signal sources with a separate ground reference, connect the ground from the signal source to an ANALOG GND (pins 18 and 20-22 on P3). Figure 2-4 shows how these connections are made. Note that you can mix single-ended with dedicated ground and differential channels by setting the individual switches on S2 to the proper position.

Connecting the Trigger In and Trigger Out Pins, Cascading Boards

The VF910 board has an external trigger input (P2-39) and output (P2-43) so that two or more boards can be cascaded and run synchronously in a "master/slave" configuration. By cascading two (or more) boards as shown in Figure 2-5, they can be triggered to start an A/D conversion at the same time. Note that when using the external trigger output (P2-43) such as on the master board in Figure 2-5, you must set the bottom jumper on P3 to TRIG.

If you apply an external trigger to the board's trigger in pin, note that the trigger can be negative- or positive-going. The pulse duration should be at least 100 nanoseconds. When using the TRIGGER OUT, the pulse must always be positive-going.

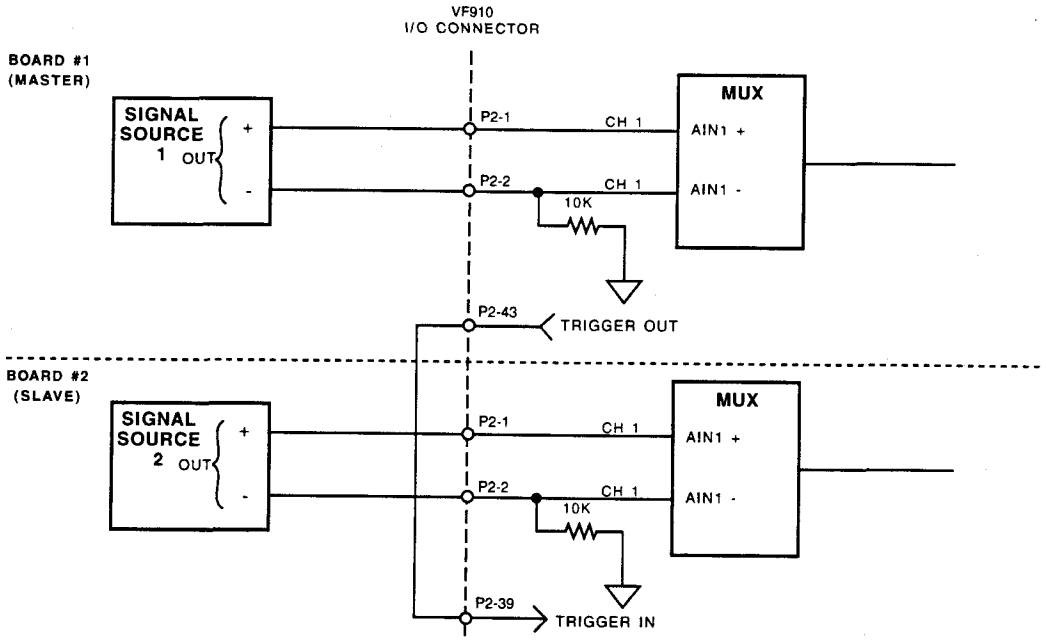


Fig. 2-5 — Cascading Two Boards for Simultaneous Sampling

Connecting the Analog Outputs

For each of the two D/A outputs, connect the high side of the device receiving the output to the AOUT channel (P2-17 or P2-19) and connect the low side of the device to an ANALOG GND (P2-18 or P2-20).

Connecting the Timer/Counters and Digital I/O

For all of these connections, the high side of an external signal source or destination device is connected to the appropriate signal pin on the I/O connector, and the low side is connected to any DIGITAL GND.

Running the 910DIAG Diagnostics Program

Now that your board is ready to use, you will want to try it out. An easy-to-use, menu-driven diagnostics program, 910DIAG, is included with your example software to help you verify your board's operation. You can also use this program to make sure that your current base address setting does not contend with another device.

CHAPTER 3

HARDWARE DESCRIPTION

This chapter describes the features of the VF910 hardware. The major circuits are the A/D which consists of the V/F converter and associated timing and counting, the D/A, and the digital I/O lines. Three timer/counters from the user 8254 are available at the I/O connector for your use. Board interrupts are also described in this chapter.

The VF910 board has three major circuits, the A/D which consists of the V/F converter and associated timing and counting, the D/A, and the digital I/O lines. Three timer/counters from the user 8254 is available at the I/O connector for your use. Figure 3-1 shows the block diagram of the board. This chapter describes hardware which makes up the major circuits. It also discusses interrupts.

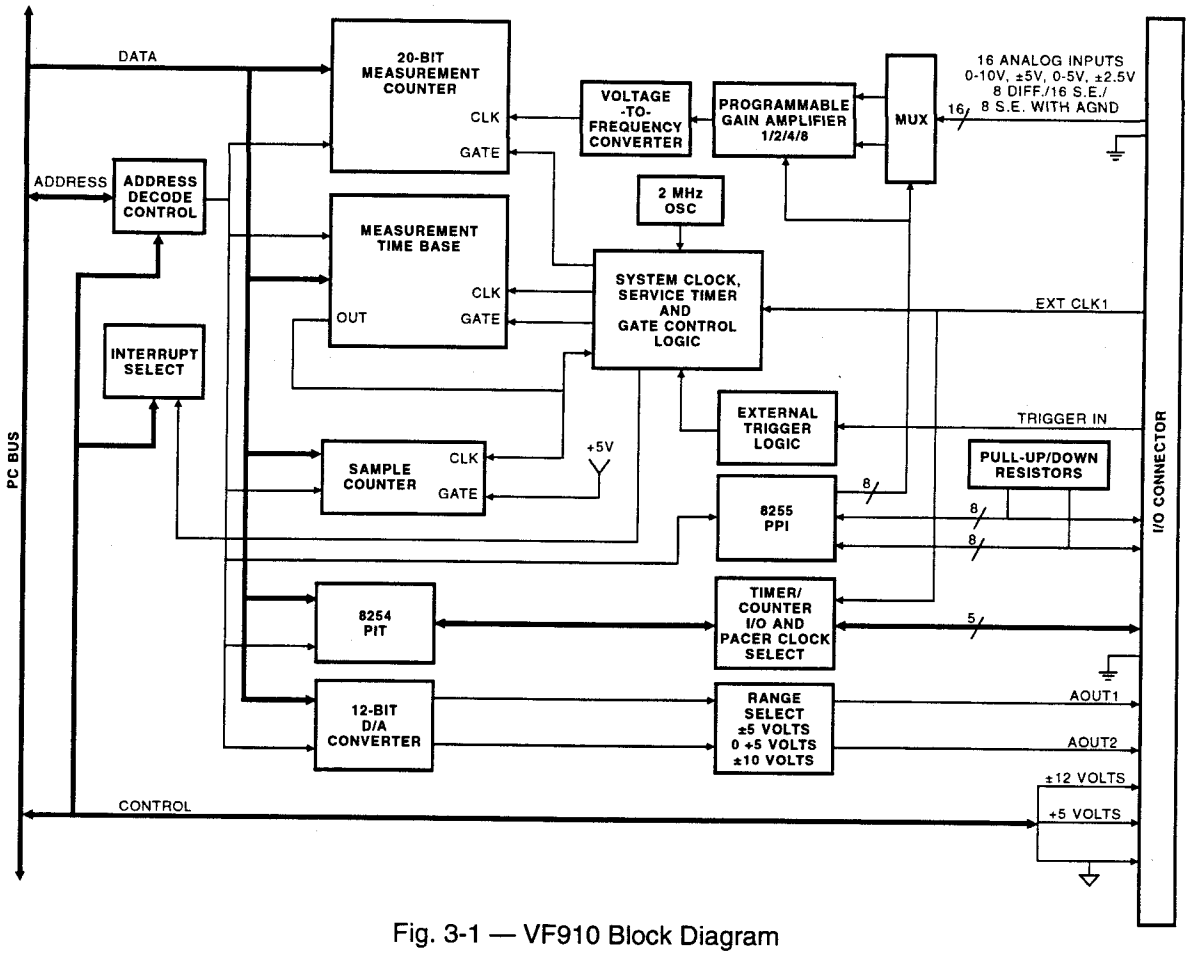


Fig. 3-1 — VF910 Block Diagram

A/D Conversion Circuitry

The VF910 board performs analog-to-digital conversions using a voltage-to-frequency converter and timing and counting circuits. This circuitry functions as an exceptionally accurate integrating converter. The V/F converter converts the input voltage to a frequency between 0 and system clock ÷ 2 (full scale), and this frequency is counted by the frequency counter for a specified period of time. The following paragraphs describe the A/D circuitry.

Analog Inputs

The input type can be set for 8 differential, 8 single-ended with dedicated ground, or 16 single-ended by opening and closing switches on DIP switch S2 and setting the jumpers on P6. You can mix differential and single-ended with dedicated ground as described in Chapter 1 under the S2 settings discussion. Single-ended operation is typically used when the analog input voltage source is close to the board and the voltage levels are fairly high (greater than ±0.5 volts). The differential mode provides noise immunity when long cable runs are unavoidable, signal levels are low, or surrounding electrical noise is high. Software programmable binary gains of 1, 2, 4, and 8 let you amplify low level signals to more closely match the board's input ranges. These gains can be customized for even greater input control by adding a gain multiplying resistor circuit as described in Chapter 1.

The input range is jumper-selectable for 5 volts or 10 volts, unipolar or bipolar. The available ranges are 0 to +5, 0 to +10, -2.5 to +2.5, and -5 to +5 volts. The board is factory set for -2.5 to +2.5 volts. Should you need to change the input range and/or polarity, you should recalibrate the board according to the instructions in Chapter 6, *Calibration*. Each channel has an input impedance of greater than 10 megohms. Overvoltage protection of ±35 Vdc is provided at the multiplexer.

V/F Converter

The V/F converter receives an input voltage and converts it to a corresponding frequency which is then read from the frequency counter as 20-bit data. The conversion time varies, depending on the degree of accuracy you want in your result and the speed of the system clock. The software selectable system clock can be set for 0.5, 1, or 2 MHz. A 1 MHz clock provides the best speed versus linearity tradeoff for most applications. At 0.5 MHz, linearity improves, but the conversion time doubles. A 2 MHz clock performs the fastest conversions, but sacrifices linearity. With a system clock of 1 MHz, a 12-bit conversion is performed in about 8 milliseconds, a 16-bit conversion in 131 milliseconds, and an 18-bit conversion in 524 milliseconds.

The V/F converter used on the VF910 is Analog Devices' AD652 monolithic synchronous V/F converter. This extremely linear device is clocked by the programmable system clock. The system clock signal is divided by 2 on the chip, resulting in the 0 to system clock ÷ 2 frequency range of the converter. The same system clock is used to gate the timer circuitry, which means that you will get accurate conversions even if the clock frequency should drift.

To compensate for gain drift in the V/F converter, a trimpot is provided on the board. Chapter 6, *Calibration*, tells you how to adjust this trimpot.

Timing and Counting Circuits

The timing and counting circuits used with the V/F converter are shown in Figure 3-2. Very simply, the 8254 opens a window of time and the 20-bit counter counts the frequency output of the V/F converter.

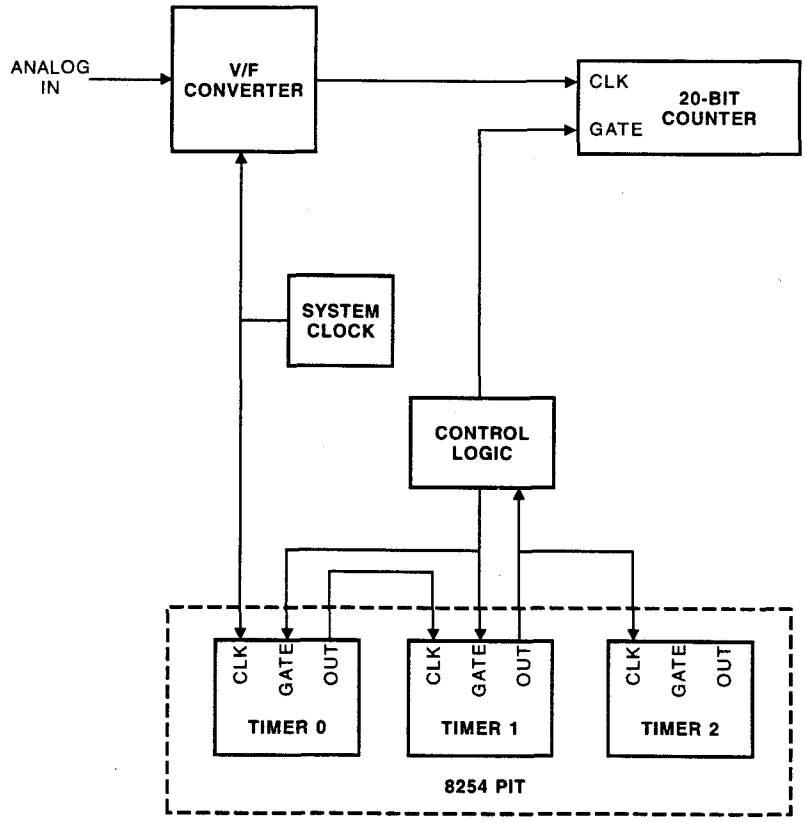


Fig. 3-2 — V/F Timing and Counting Block Diagram

The 20-bit counter has two flags: counter overflow and measurement overflow. The counter overflow flag is set if the 20-bit counter overflows within a single measurement cycle. The measurement overflow flag is set if two or more measurement cycles have been executed without the counter being cleared between cycles.

As shown in Figure 3-2, the 8254 programmable interval timer (PIT) contains three 16-bit timers. Two of these timers are cascaded to form a 32-bit timer which gates the frequency counters. The frequency counters are opened for a window of time specified by this 32-bit timer. You program the timer for the amount of time that you want the frequency counters to count, according to your desired resolution. The remaining timer in the 8254 (timer 2) is the sample counter. The 8254 data sheet is included in Appendix C to assist you in using this timer.

A 20-bit counter is used to count the frequency output of the V/F converter for the period specified by the 8254 timer. For single conversions, a conversion is started, the 20-bit counter is gated for a specified period of time, and the value is read. For continuous conversions, the first conversion is started, the 20-bit counter is gated for a specified period of time, and, when the conversion is ready, the programmable service counter starts its countdown during which the converted data is read and the input channel and gain for the next conversion are set. When the service counter reaches 0, the next conversion is triggered.

D/A Converter

Two independent 12-bit analog output channels are included on the VF910. The analog outputs are generated by two 12-bit D/A converters with independent jumper-selectable output ranges of ±5, ±10, 0 to +5, and 0 to +10 volts. The ±10 volt range has a resolution of 4.88 millivolts, the ±5 and 0 to +10 volt ranges have a resolution of 2.44 millivolts, and the 0 to +5 volt range has a resolution of 1.22 millivolts. The D/A outputs can be updated simultaneously or asynchronously.

Timer/Counters

Three 16-bit, 8 MHz timer/counters on the user 8254, TC0, TC1, and TC2, support a wide range of timing and counting functions. Each timer/counter has two inputs, CLK and GATE, and one output, OUT. Figure 3-3 shows the timer/counter circuitry and the connections you can make to the inputs and outputs. Each timer/counter can be programmed as binary or BCD down counters by writing the appropriate data to the command word, as described in Chapter 4. The command word also lets you set up the mode of operation. The six programmable modes are:

Mode 0	Event Counter (Interrupt on Terminal Count)
Mode 1	Hardware-Retriggerable One-Shot
Mode 2	Rate Generator
Mode 3	Square Wave Mode
Mode 4	Software-Triggered Strobe
Mode 5	Hardware Triggered Strobe (Retriggerable)

These modes are detailed in the 8254 Data Sheet, reprinted from Intel in Appendix C.

Digital I/O, Programmable Peripheral Interface

The 8255 programmable peripheral interface (PPI) is used for digital I/O functions. This high-performance TTL/CMOS compatible chip has 24 digital I/O lines divided into two groups of 12 lines each:

Group A — Port A (8 lines) and Port C Upper (4 lines);
Group B — Port B (8 lines) and Port C Lower (4 lines).

Port A and Port C are available at the external I/O connector, P2. Port B is dedicated to on-board functions and is not available for your use. You can use the 16 lines of Ports A and C in one of these three PPI operating modes:

Mode 0 — Basic input/output. Lets you use simple input and output operation for a port. Data is written to or read from the specified port.

Mode 1 — Strobed input/output. Lets you transfer I/O data from Port A in conjunction with strobes or handshaking signals.

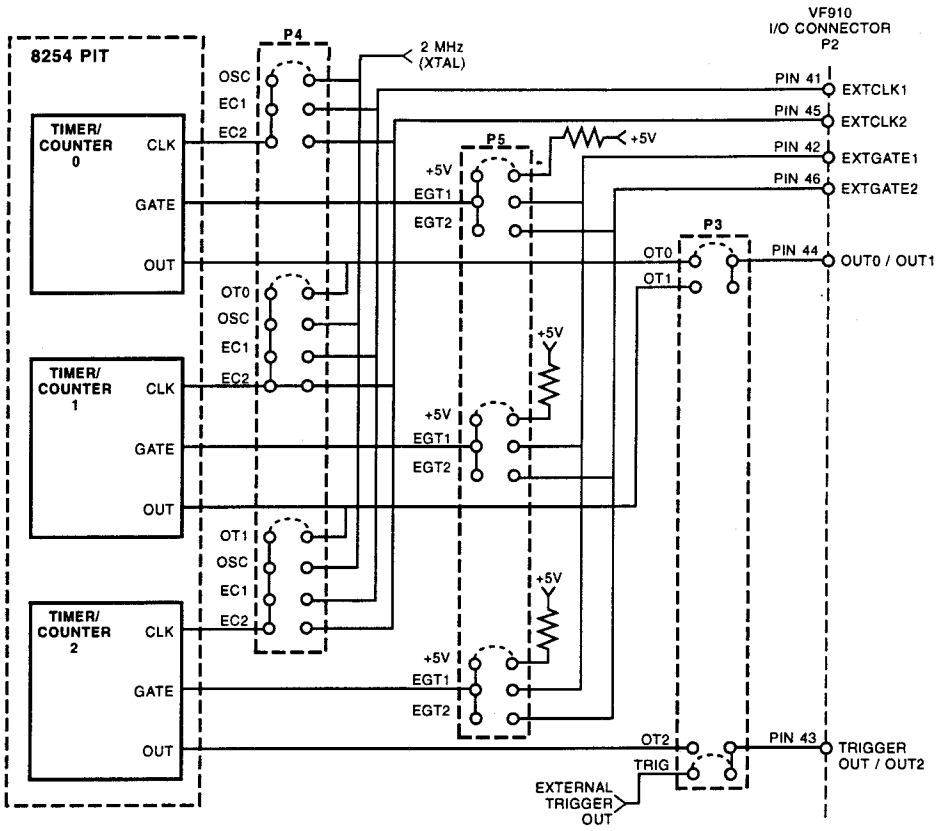


Fig. 3-3 — User 8254 Timer/Counter Circuitry

Mode 2 — Strobed bidirectional input/output. Lets you communicate bidirectionally with an external device through Port A. Handshaking is similar to Mode 1.

These modes are detailed in the 8255 Data Sheet, reprinted from Intel in Appendix C.

Interrupts

The VF910 has two software selectable interrupt sources: end-of-convert and external trigger. The end-of-convert (EOC) line can be used to interrupt the computer when a conversion is completed. When the 32-bit timer's count reaches 0, the counter gate closes, the conversion is complete, and the EOC line goes high. When in the continuous convert mode, the service time begins, and you can read the data, change the channel/gain settings, and reset the 20-bit counter. The EOC line can be connected through software, as shown in the I/O Map discussion in Chapter 4. On power-up, the EOC line is disabled. Change the IRQ channel if necessary for your application. If you connect the end-of-convert to one of the interrupt channels, an interrupt will occur when the line transitions from low (converting) to high (not converting). The external trigger line (trigger in, P2-39) can be used to feed in an external interrupt signal or loop a signal back onto the board, such as the output of timer/counter 2, to be used as an interrupt. When using the external trigger line as an external interrupt signal, the polarity (interrupt on rising or falling edge) is set at BA + 21, bit 1. We recommend that you have an understanding of how to use interrupts in your system before you connect the end-of-convert to an IRQ channel.

CHAPTER 4

BOARD OPERATION AND PROGRAMMING

This chapter tells you how to initialize the board and read the converted data. It describes operating modes and provides flow diagrams and a complete description of the I/O map to aid you in programming your VF910 board. The example programs included on the disk in your board package are listed at the end of this chapter. These programs, written in BASIC, Turbo Pascal, and Turbo C, include source code to simplify your applications programming.

Chapter 5, *Calculating Frequencies, Voltages, and Bits*, contains tables, formulas, and examples to help you understand the principles of V/F conversion.

Defining the I/O Map

The I/O map for the VF910 is shown in Table 4-1 below. As shown, the board occupies 23 consecutive I/O port locations. The base address (designated as BA) can be selected using DIP switch S1 as described in Chapter 1, *Board Settings*. This switch can be accessed without removing the board from the computer. S1 is factory set at 300 hex (768 decimal). The following sections describe the register contents of each address used in the I/O map.

Table 4-1 — VF910 I/O Map

Register Description	Read Function	Write Function	Address * Decimal / (Hex)
A/D Data Low Byte	Read bottom 8 bits of 20-bit converted data word	Reserved	BA + 0 / (00)
A/D Data Middle Byte	Read middle 8 bits of 20-bit converted data word	Reserved	BA + 1 / (01)
A/D Data High Byte/Status	Read top 4 bits of 20-bit converted data word & status	Reserved	BA + 2 / (02)
Board Ready/Clear 20-bit Conversion Counter	Read board ready code	Clear the 20-bit conversion counter	BA + 3 / (03)
8254 Timer/Counter 0	Read count value	Load count register	BA + 4 / (04)
8254 Timer/Counter 1	Read count value	Load count register	BA + 5 / (05)
8254 Timer/Counter 2	Read count value	Load count register	BA + 6 / (06)
8254 Control Register	Reserved	Program 8254 mode	BA + 7 / (07)
8255 PPI Port A Digital I/O	Read 8-bit Port A digital input lines	Program 8-bit Port A digital output lines	BA + 8 / (08)
8255 PPI Port B (A/D Channel/Gain Select)	Read channel/gain settings	Program channel & gain	BA + 9 / (09)
8255 PPI Port C Digital I/O	Read 8-bit Port C digital input lines	Program 8-bit Port C digital output lines	BA + 10 / (0A)
8255 PPI Control Register	Reserved	Program 8255 configuration	BA + 11 / (0B)
DAC 1 Low Byte	Reserved	Program bottom 8 bits of 12-bit DAC 1 data	BA + 12 / (0C)
DAC 1 High Byte	Reserved	Program top 4 bits of 12-bit DAC 1 data	BA + 13 / (0D)
DAC 2 Low Byte	Reserved	Program bottom 8 bits of 12-bit DAC 2 data	BA + 14 / (0E)
DAC 2 High Byte	Reserved	Program top 4 bits of 12-bit DAC 2 data	BA + 15 / (0F)
8254 User Timer/Counter 0	Read count value	Load count register	BA + 16 / (10)
8254 User Timer/Counter 1	Read count value	Load count register	BA + 17 / (11)
8254 User Timer/Counter 2	Read count value	Load count register	BA + 18 / (12)
8254 Control Register	Reserved	Program 8254 mode	BA + 19 / (13)
Board Setup	Reserved	Program system clock, conversion mode and interrupt channel	BA + 20 / (14)
A/D Trigger Mode	Reserved	Program trigger mode and parameters	BA + 21 / (15)
Reset/Update DACs	Resets board	Simultaneously update DAC 1 and DAC 2	BA + 22 / (16)

* BA = Base Address

BA + 0: A/D Data Low Byte (Read Only)

A read provides the low byte (bits 0 through 7) of the 20-bit converted data in the conversion counter.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

BA + 1: A/D Data Middle Byte (Read Only)

A read provides the middle byte (bits 8 through 15) of the 20-bit converted data in the conversion counter.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
D7	D6	D5	D4	D3	D2	D1	D0

BA + 2: A/D Data High Byte (Read Only)

A read provides the high byte (bits 16 through 19) of the 20-bit converted data in the conversion counter, plus the counter overflow, measurement overflow, and conversion ready flag status. The counter overflow tells you if the 20-bit conversion counter overflows during a measurement cycle. The measurement overflow flag tells you if two or more measurement cycles are executed without clearing the counter between executions. The conversion ready flag tells you the conversion status (conversion running or conversion finished).

		X		Bit 19	Bit 18	Bit 17	Bit 16
D7	D6	D5	D4	D3	D2	D1	D0

A/D Conversion Status
0 = conversion running
1 = conversion complete

Measurement Overflow
0 = measurements OK
1 = 2 or more measurements without counter reset

Counter Overflow
0 = no overflow
1 = overflow

BA + 3: Board Ready/Clear 20-bit Conversion Counter (Read/Write)

A read must give you the value of 82 (52 hex) to indicate that the BA is set properly. A write clears the 20-bit conversion counter and flags. The data written is irrelevant.

BA + 4: 8254 Timer/Counter 0 (Read/Write)

Two reads show the count in the timer/counter, and two writes load the counter/timer with a new 16-bit value, LSB followed by MSB. The timer/counter must be loaded in two 8-bit steps. Counting begins as soon as the MSB is loaded.

This timer/counter, cascaded with timer/counter 1 to form a 32-bit timer, generates the board's internal pacer clock which controls measurements and starts and stops conversions.

BA + 5: 8254 Timer/Counter 1 (Read/Write)

Two reads show the count in the timer/counter, and two writes load the counter/timer with a new 16-bit value, LSB followed by MSB. The timer/counter must be loaded in two 8-bit steps. Counting begins as soon as the MSB is loaded.

This timer/counter, cascaded with timer/counter 0 to form a 32-bit timer, generates the board's internal pacer clock which controls measurements and starts and stops conversions.

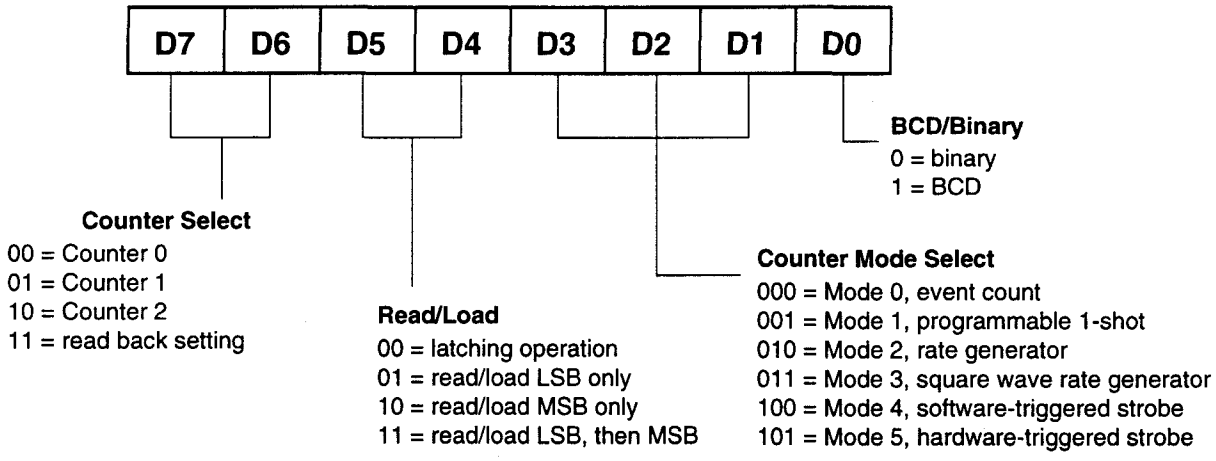
BA + 6: 8254 Timer/Counter 2 (Read/Write)

Two reads show the count in the timer/counter, and two writes load the counter/timer with a new 16-bit value, LSB followed by MSB. The timer/counter must be loaded in two 8-bit steps. Counting begins as soon as the MSB is loaded.

This timer/counter, with its clock input connected to the output of timer/counter 1, can be used as a sample counter to provide a hardware count of the number of samples being taken.

BA + 7: 8254 Control Word (Write Only)

Accesses the 8254 PIT control register to directly control the three timer/counters.



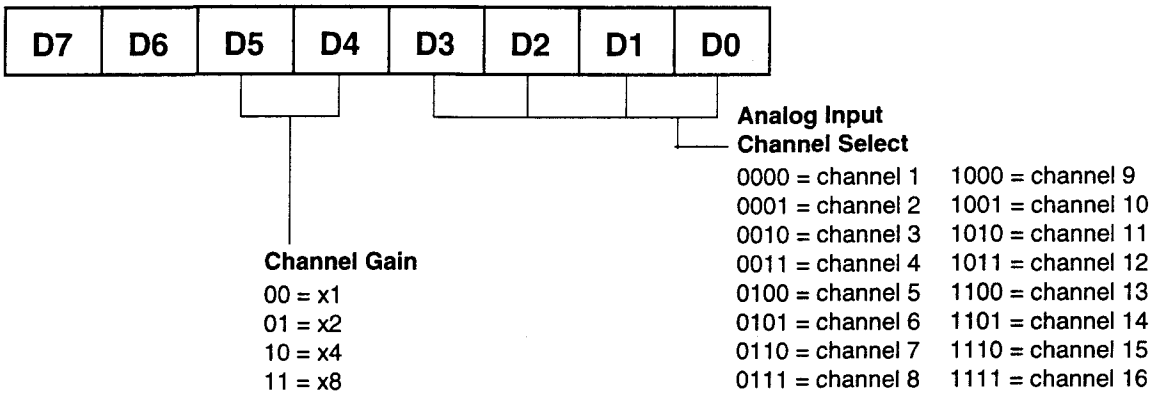
BA + 8: PPI Port A — Digital I/O (Read/Write)

Transfers the 8-bit Port A digital input and digital output data between the board and an external device. A read transfers data from the external device, through P2, and into PPI Port A; a write transfers the written data from Port A through P2 to an external device.

BA + 9: PPI Port B — Channel/Gain Select (Read/Write)

A write programs the analog input channel and gain for the next conversion. This port must be set up as a Mode 0 output for proper operation.

Reading this register shows you the current bit settings.

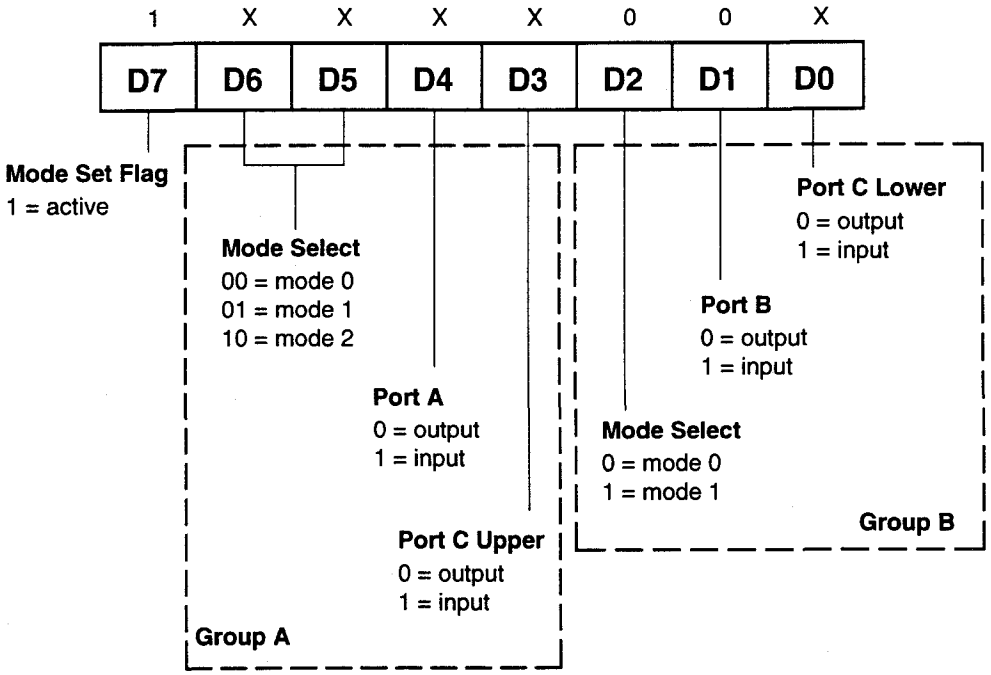


BA + 10: PPI Port C — Digital I/O (Read/Write)

Transfers the two 4-bit Port C digital input and digital output data groups (Port C Upper and Port C Lower) between the board and an external device. A read transfers data from the external device, through P2, and into PPI Port C; a write transfers the written data from Port C through P2 to an external device.

BA + 11: 8255 PPI Control Word (Write Only)

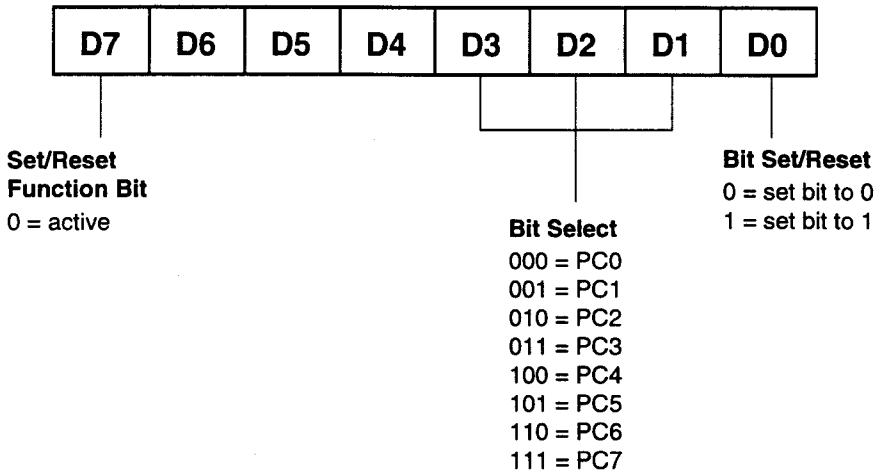
When bit 7 of this word is set to 1, a write programs the PPI configuration. The PPI must be programmed so that Port B is a Mode 0 output port, as shown below (X = don't care).



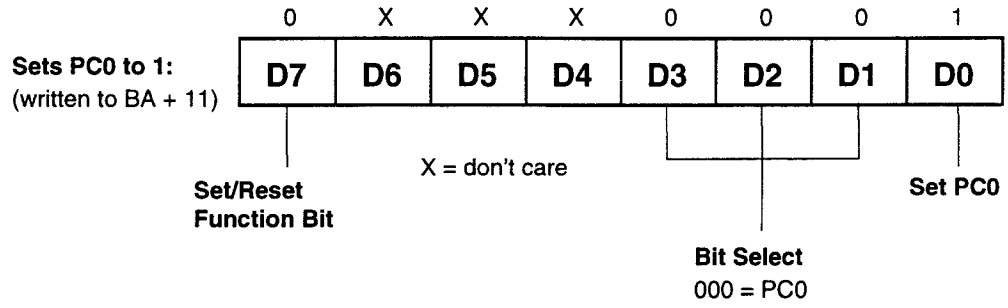
The table below shows the control words for the 16 possible Mode 0 Port I/O combinations. The control words which set Port B as an input cannot be used on the VF910.

8255 Port I/O Flow Direction and Control Words, Mode 0						
Group A		Group B		Control Word		
Port A	Port C Upper	Port B	Port C Lower	Binary	Decimal	Hex
Output	Output	Output	Output	1 0 0 0 0 0 0 0	128	80
Output	Output	Output	Input	1 0 0 0 0 0 0 1	129	81
Output	Output	Input	Output	1 0 0 0 0 0 1 0	130	82
Output	Output	Input	Input	1 0 0 0 0 0 1 1	131	83
Output	Input	Output	Output	1 0 0 0 1 0 0 0	136	88
Output	Input	Output	Input	1 0 0 0 1 0 0 1	137	89
Output	Input	Input	Output	1 0 0 0 1 0 1 0	138	8A
Output	Input	Input	Input	1 0 0 0 1 0 1 1	139	8B
Input	Output	Output	Output	1 0 0 1 0 0 0 0	144	90
Input	Output	Output	Input	1 0 0 1 0 0 0 1	145	91
Input	Output	Input	Output	1 0 0 1 0 0 1 0	146	92
Input	Output	Input	Input	1 0 0 1 0 0 1 1	147	93
Input	Input	Output	Output	1 0 0 1 1 0 0 0	152	98
Input	Input	Output	Input	1 0 0 1 1 0 0 1	153	99
Input	Input	Input	Output	1 0 0 1 1 0 1 0	154	9A
Input	Input	Input	Input	1 0 0 1 1 0 1 1	155	9B

When bit 7 of the PPI control word is set to 0, a write can be used to individually program the Port C lines.



For example, if you want to set Port C bit 0 to 1, you would set up the control word so that bit 7 is 0; bits 1, 2, and 3 are 0 (this selects PC0); and bit 0 is 1 (this sets PC0 to 1). The control word is set up like this:



BA + 12: D/A Converter 1 LSB (Read/Write)

A write programs the DAC1 LSB (eight bits).

BA + 13: D/A Converter 1 MSB (Read/Write)

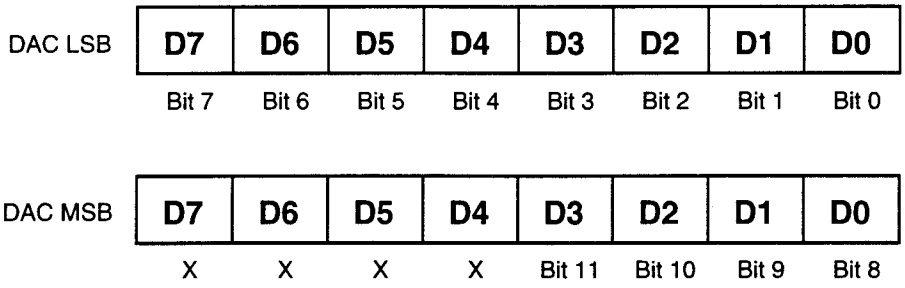
A write programs the DAC1 MSB (four bits) into D0 through D3; D4 through D7 are irrelevant.

BA + 14: D/A Converter 2 LSB (Read/Write)

A write programs the DAC2 LSB (eight bits).

BA + 15: D/A Converter 2 MSB (Read/Write)

A write programs the DAC2 MSB (four bits) into D0 through D3; D4 through D7 are irrelevant.



BA + 16: User 8254 Timer/Counter 0 (Read/Write)

Two reads show the count in the timer/counter, and two writes load the counter/timer with a new 16-bit value, LSB followed by MSB. The timer/counter must be loaded in two 8-bit steps. Counting begins as soon as the MSB is loaded.

BA + 17: User 8254 Timer/Counter 1 (Read/Write)

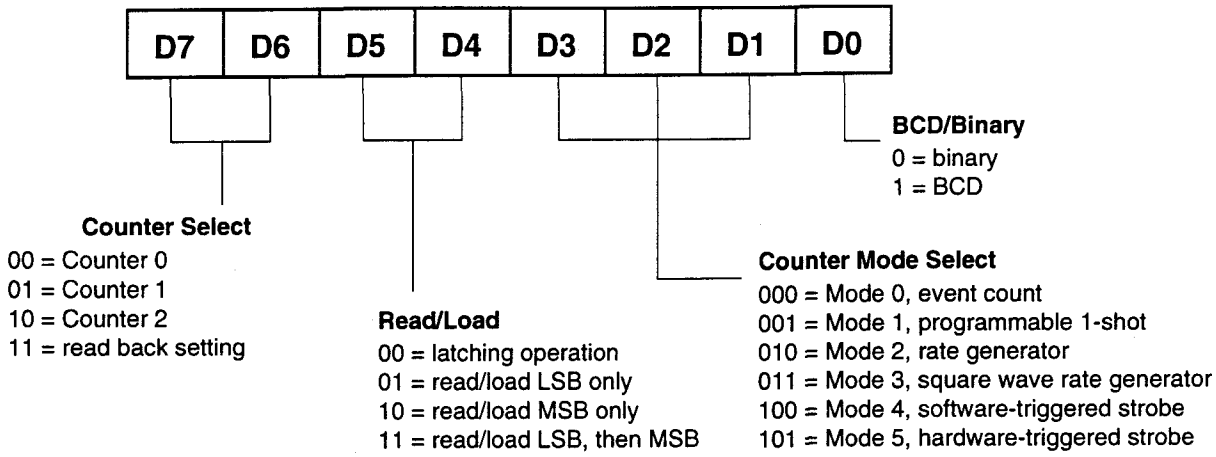
Two reads show the count in the timer/counter, and two writes load the counter/timer with a new 16-bit value, LSB followed by MSB. The timer/counter must be loaded in two 8-bit steps. Counting begins as soon as the MSB is loaded.

BA + 18: User 8254 Timer/Counter 2 (Read/Write)

Two reads show the count in the timer/counter, and two writes load the counter/timer with a new 16-bit value, LSB followed by MSB. The timer/counter must be loaded in two 8-bit steps. Counting begins as soon as the MSB is loaded.

BA + 19: User 8254 Control Word (Write Only)

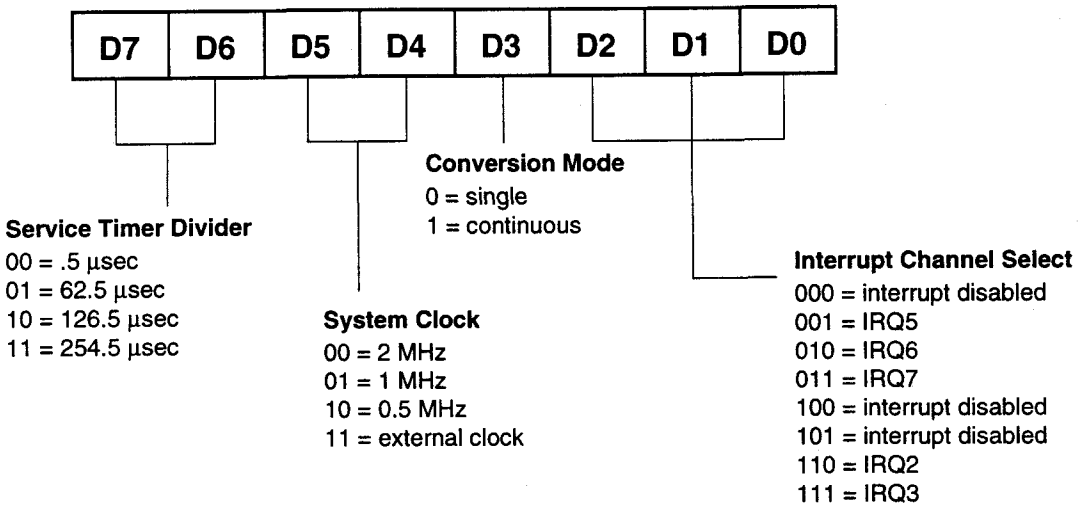
Accesses the 8254 PIT control register to directly control the three user timer/counters.



BA + 20: Board Setup Register (Write Only)

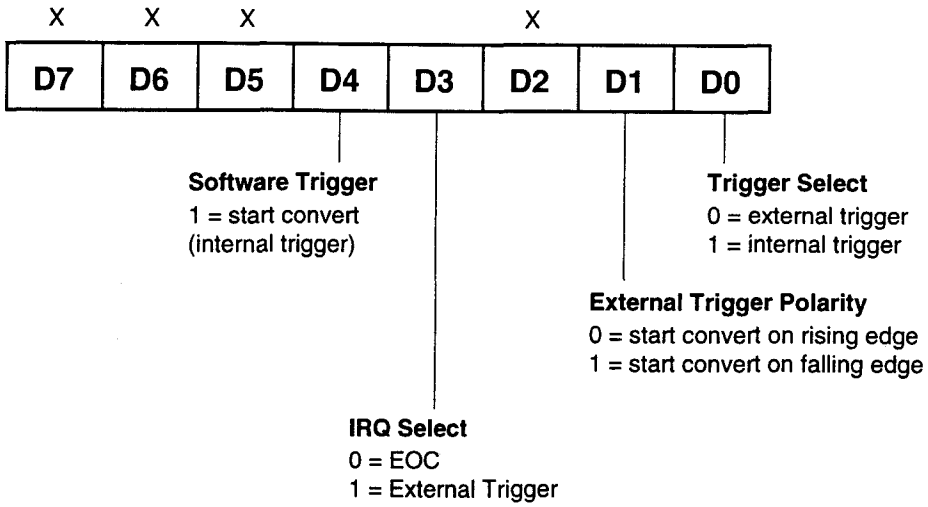
A write sets the PC's interrupt channel, the A/D conversion mode, the system clock speed, and the service timer divider. Bits 0 through 2 are used to select the interrupt channel. Three settings, 000, 100, and 101, disable the interrupt. If an IRQ channel is programmed, the interrupt selected at BA + 21 is automatically enabled on that channel.

The service time is programmable to provide you with as much time as you need to read the data, clear the counter, and change the channel and gain.



BA + 21: A/D Trigger Mode Register (Write Only)

This register sets up various triggering parameters for conversions. Bit 0 sets the trigger mode, internal or external. In the external trigger mode, a conversion can be started on the rising or falling edge of the trigger, depending on the setting of bit 1. Bit 3 sets the interrupt source. Bit 4 can be used to start a conversion in internal trigger mode. In the single conversion mode, only one measurement is taken. In the continuous mode, after the start, the board is continuously converting.


X X X X
D7 D6 D5 D4 D3 D2 D1 D0
Software Trigger
1 = start convert
(internal trigger)
Trigger Select
0 = external trigger
1 = internal trigger
External Trigger Polarity
0 = start convert on rising edge
1 = start convert on falling edge
IRQ Select
0 = EOC
1 = External Trigger

BA + 22: Reset/Update DACs (Read/Write)

A read resets the board. The data written is irrelevant.

A write simultaneously updates the two D/A outputs with the latched data. If the data written to either channel has not been updated since the last conversion, the output of the corresponding DAC will not change.

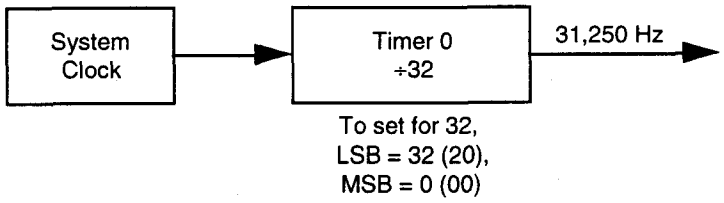
A/D Conversions

Before you can start taking A/D conversions, you must clear the 20-bit counter and program the 8254 timer. The software provided with your board contains example programs for board initialization.

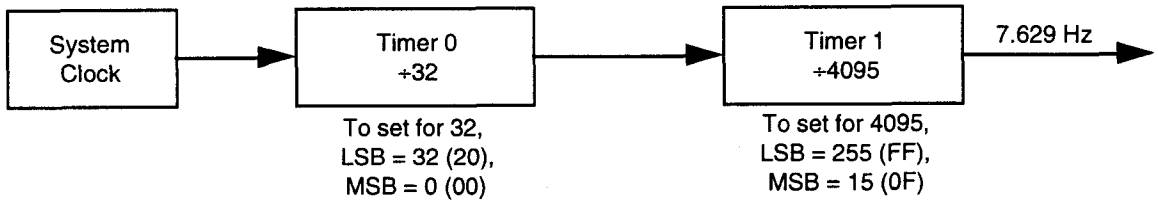
You can monitor the conversion status using the end-of-convert bit at I/O address location BA + 2. When bit 7 of this word is low, a conversion is in progress. When it goes high, the conversion is completed. Note that the end-of-convert line can also be monitored through a software programmable IRQ line if it is enabled.

Programming the 8254 Timer

Two of the 8254's 16-bit timers are cascaded to form a 32-bit timer which gates the 20-bit conversion counter. The timer is clocked by the same system clock which supplies the V/F converter. Timer 0 and timer 1 are programmed with the values that will open the conversion gate for the desired time window. In the example programs included with your board, timer 0 is always set at 32. This divides the input frequency of system clock by 32, which produces an output frequency of system clock ÷ 32 going into timer 1. For a system clock of 1 MHz, this is:



Then, timer 1 is programmed with the correct divider value to take readings at the desired resolution. For example, if you want a resolution of 16 bits with the system clock programmed to run at 1 MHz, then you must program timer 1 to further divide the output of timer 0 by 4095. This produces an output frequency of 7.629 Hz, which will open the 20-bit conversion counter gate for 131.072 milliseconds giving you a 16-bit resolution:



NOTE: The above example is for both single and continuous conversions. Note that you must always subtract 1 from the value you load into timer 1 in order to have an accurate count. This is done to compensate for how the 8254 handles single countdown operations for cascaded timers. In the continuous mode, the sampling rate is determined by:

fs = 1 ÷ (gate time + service time).

As you can see, the timing calculations can be somewhat complex. The formulas for calculating the counts to load into the timers are given in Chapter 5. Chapter 5 also provides tables and formulas for decimal counts. These are helpful for voltage-based resolutions, such as a resolution of 100 microvolts. Here, you can refer to the following table to help you determine the count to be loaded into the timers for bit-based resolutions.

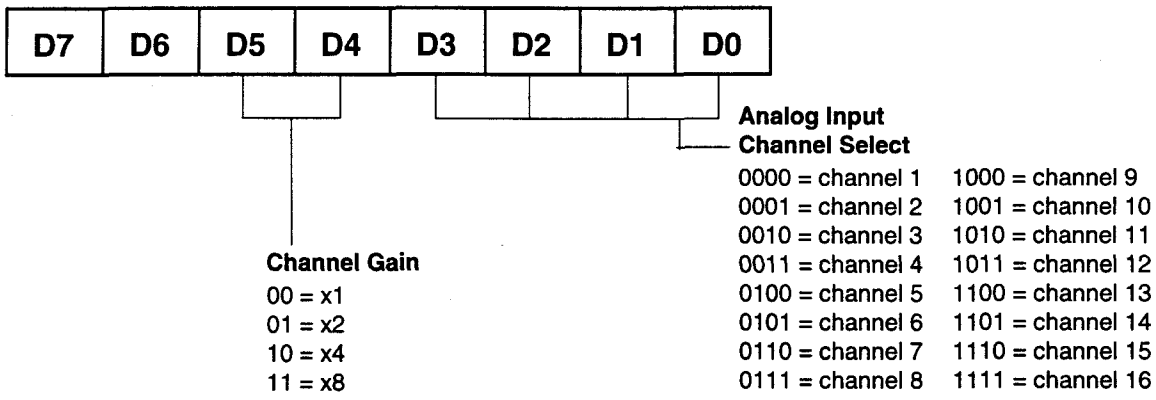
Resolution	Timer 0 LSB (Decimal/Hex)	Timer 0 MSB (Decimal/Hex)	Timer 1 LSB (Decimal/Hex)	Timer 1 MSB (Decimal/Hex)
12 bits	32 / 20	0 / 00	255 / FF	0 / 00
13 bits	32 / 20	0 / 00	255 / FF	1 / 01
14 bits	32 / 20	0 / 00	255 / FF	3 / 03
15 bits	32 / 20	0 / 00	255 / FF	7 / 07
16 bits	32 / 20	0 / 00	255 / FF	15 / 0F
17 bits	32 / 20	0 / 00	255 / FF	31 / 1F
18 bits	32 / 20	0 / 00	255 / FF	63 / 3F

This chapter's final example for the 8254 timer is a portion of an initialization program, written in BASIC, which shows you how to set up the 8254 timers 0 and 1 so that they open the conversion counter for a time period of 131.072 milliseconds, giving you a 16-bit resolution with a 1 MHz system clock. The timer 1 divider is 4095. In this example, TWC stands for the 8254 control register which is addressed at BA + 7 (decimal), TA stands for timer 0 which is addressed at BA + 4, and TB stands for timer 1 which is addressed at BA + 5. All values are in hex.

```
OUT TWC, &H34      'SET UP TIMER 0 AS MODE 2
OUT TWC, &H74      'SET UP TIMER 1 AS MODE 2
OUT TA, &H20       'SET TIMER 0 DIVIDER LSB (LSB = 32 FOR DIVIDER OF 32)
OUT TA, &H0        'SET TIMER 0 DIVIDER MSB (MSB = 0 FOR DIVIDER OF 0)
OUT TB, &HFF       'SET TIMER 1 DIVIDER LSB (LSB = 255 FOR DIVIDER OF 255)
OUT TB, &HF        'SET TIMER 1 DIVIDER MSB (MSB = 15 FOR DIVIDER OF 15)
```

Initializing the 8255 PPI

The eight Port B lines of the 8255 PPI control the channel and gain selection. Port B is programmed at I/O address location BA + 9:



To use Port B for these functions, the 8255 must be initialized so that Port B is set up as a Mode 0 output port. This is done by writing this data to the PPI control word at I/O address BA + 11 (X = don't care):

1	X	X	X	X	0	0	X
D7	D6	D5	D4	D3	D2	D1	D0

Clearing the Board

It is good practice to start your program by resetting the board. You can do this by performing a read of the RESET port at BA + 22.

Setting the Channel

To select a conversion channel, you must assign the appropriate values to bits 0 through 3 at BA + 9. The table below shows you how to determine the bit settings. Note that in the single convert mode, if you don't want to change the gain setting when programming a new channel setting, you must preserve the gain portion of the channel-gain data when you set the channel.

x	x	x	x	CH3	CH2	CH1	CH0	BA + 9

Channel	CH3	CH2	CH1	CH0	Channel	CH3	CH2	CH1	CH0
1	0	0	0	0	9	1	0	0	0
2	0	0	0	1	10	1	0	0	1
3	0	0	1	0	11	1	0	1	0
4	0	0	1	1	12	1	0	1	1
5	0	1	0	0	13	1	1	0	0
6	0	1	0	1	14	1	1	0	1
7	0	1	1	0	15	1	1	1	0
8	0	1	1	1	16	1	1	1	1

Setting the Gain

To select the gain (1, 2, 4, or 8), you must assign the appropriate values to bits 4 and 5 at BA + 9. The table below shows you how to determine the bit settings. Note that in the single convert mode, if you don't want to change the channel setting when programming a new gain setting, you must preserve the channel portion of the channel-gain data when you set the gain.

x	x	G1	G0	x	x	x	x	BA + 9

Gain	G1	G0
1	0	0
2	0	1
4	1	0
8	1	1

Conversion Modes

The A/D circuitry can perform conversions in two modes, *Single Convert* and *Continuous Convert*. The board is typically used in the *Continuous Convert* mode.

- **Single Convert Mode**

The *Single Convert* mode lets you perform a single A/D conversion each time you write a 1 to the Software Trigger (Start Convert) bit, bit 4 at BA + 21. BA + 20, bit 3 should be set to 0 for single conversions. Figure 4-1 shows the timing diagram for this mode, and Figure 4-2 provides a flow diagram.

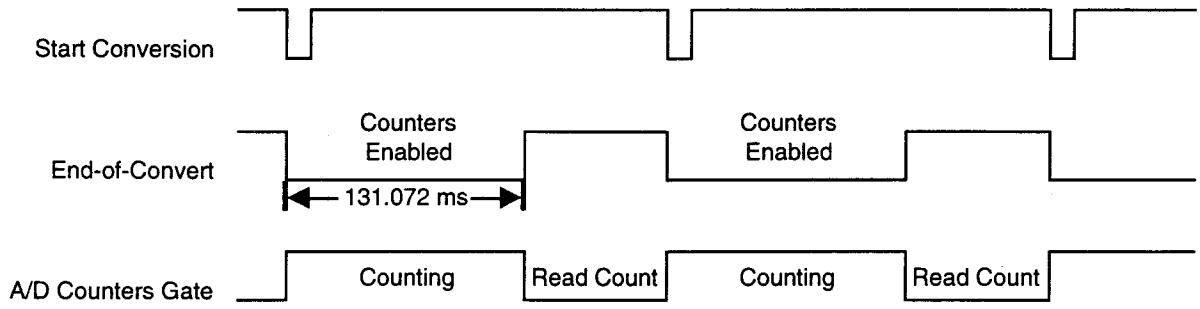


Fig. 4-1 — Single Convert Mode Timing Diagram

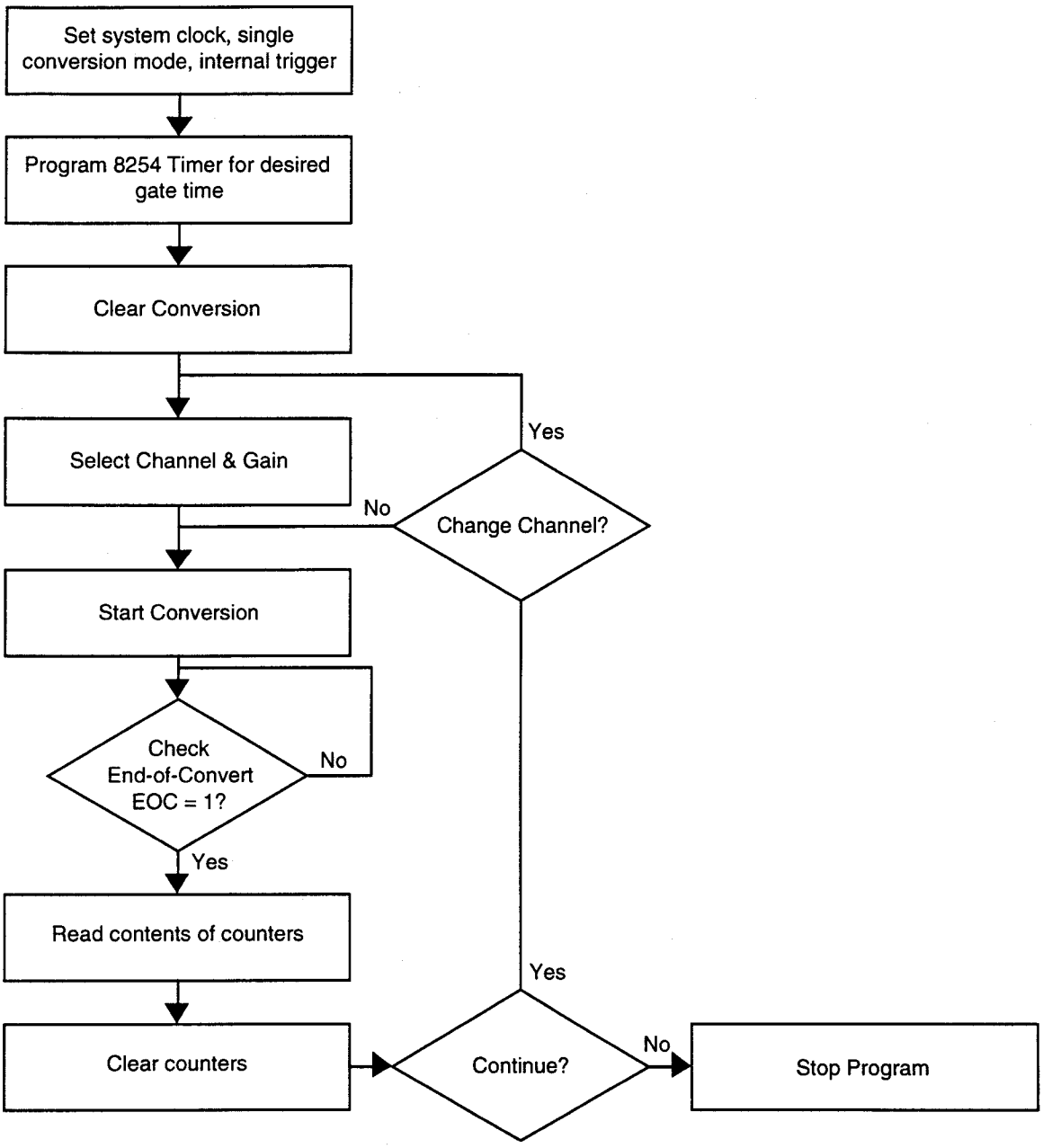


Fig. 4-2 — Single Convert Mode Flow Diagram

- **Continuous Convert Mode**

The *Continuous Convert* mode lets you perform continuous conversions by writing a 1 to the Software Trigger (Start Convert) bit, bit 4 at BA + 21. BA + 20, bit 3 should be set to 1 for continuous conversions. Figure 4-3 shows the timing diagram for this mode, and Figure 4-4 provides a flow diagram.

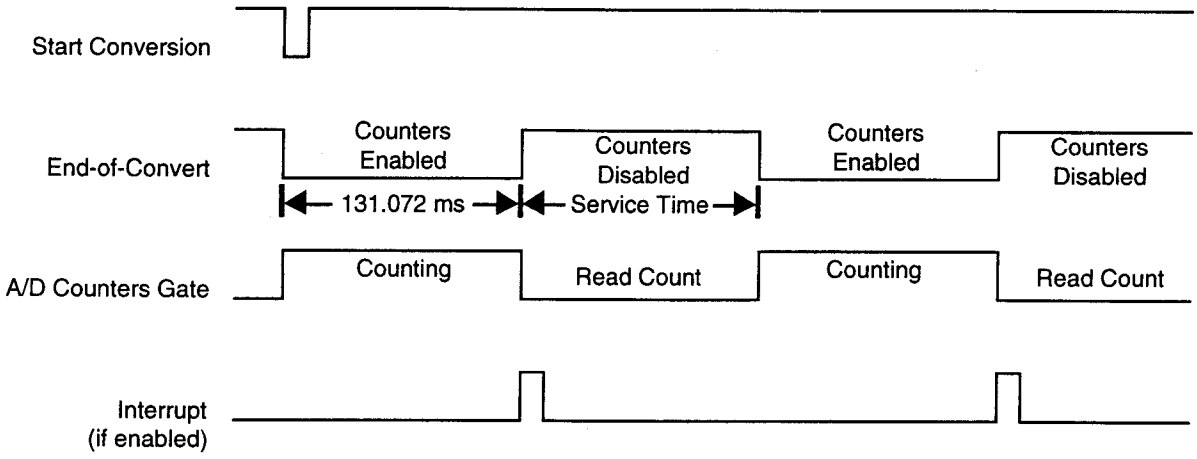


Fig. 4-3 — Continuous Convert Mode Timing Diagram

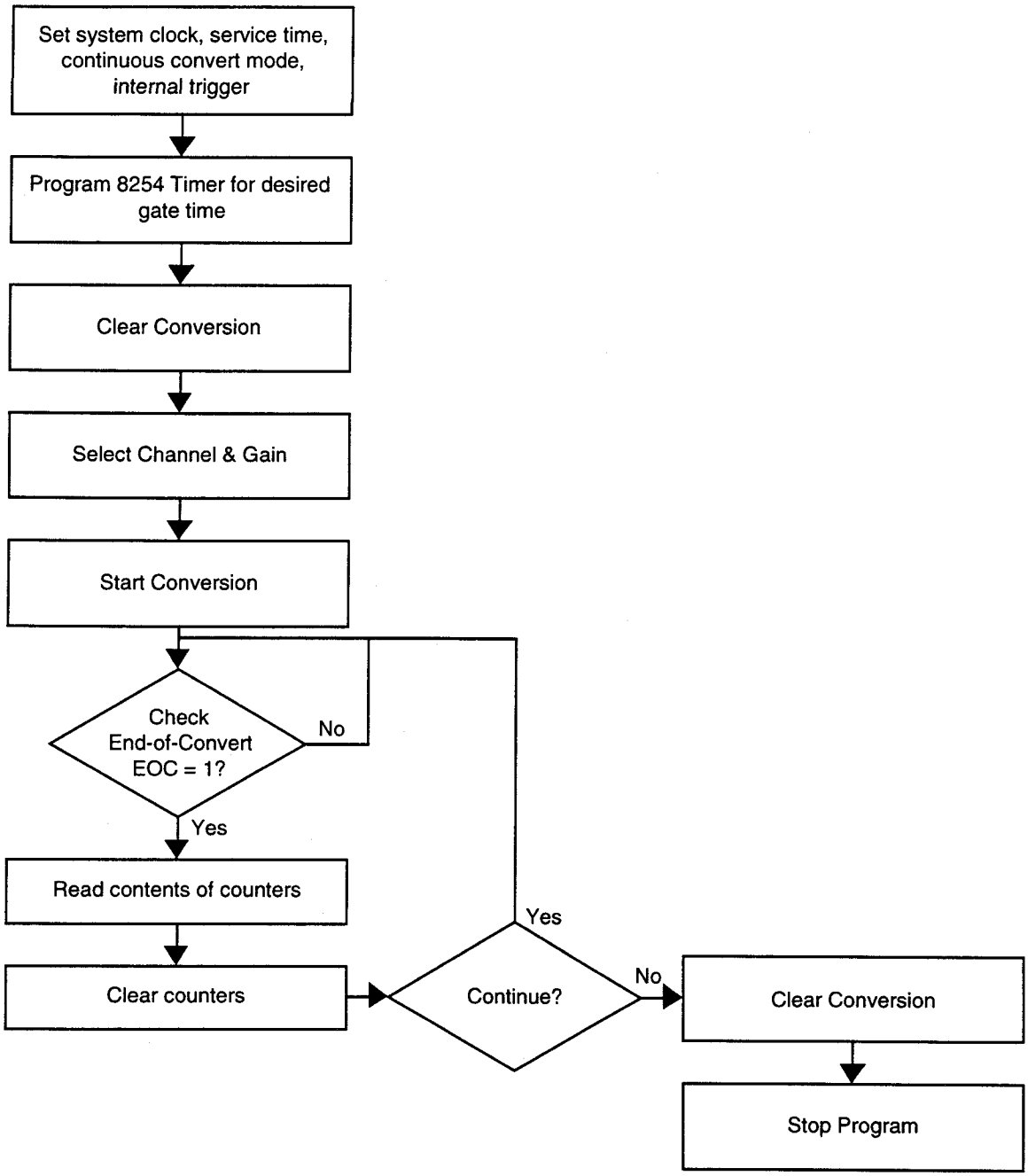


Fig. 4-4 — Continuous Convert Mode Flow Diagram

- **Cascading Boards**

Two or more boards can be cascaded and triggered so that conversions are performed simultaneously on each board. Figure 4-5 provides a flow diagram for cascaded operation. Chapter 2 shows how to connect the boards for simultaneous triggering.

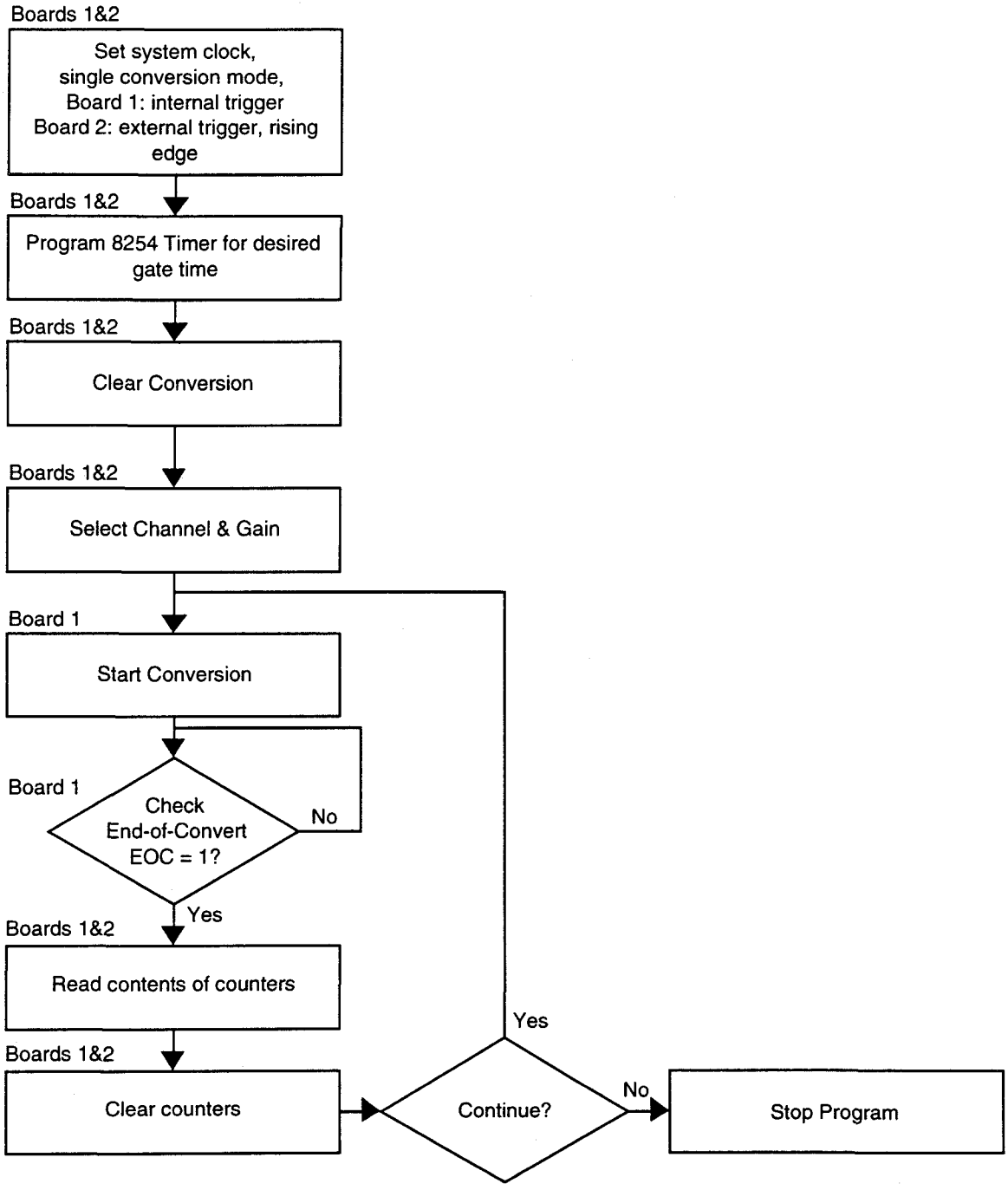


Fig. 4-5 — Cascaded Boards, Single Convert Mode Flow Diagram

Reading the Converted Data

After a conversion is completed, the data is read from the 20-bit conversion counter. The excerpt below from an example BASIC program shows you how data is read from the counter. The data is read in three bytes, the low, middle, and high byte, at three I/O address locations, BA + 0, BA + 1, and BA + 2. The upper half of the byte contains the status bit of the measurement. You must mask this bit out before using the value.

```
ADLB = INP(BA)                'READ COUNTER LOW BYTE
ADMB = INP(BA + 1)            'READ COUNTER MIDDLE BYTE
ADHB = INP(BA + 2) AND 0HE 'READ COUNTER HIGH BYTE
RESULT = ((ADLB + (ADMB x 256) + (ADHB x 65536)) x CF
```

The last line of this example program shows you how to convert the result into the true frequency output by the V/F converter. After performing the multiplication by the bit weight for each of the four bytes read, you must then multiply the result by a correction factor, CF, in order to find the true frequency of the signal you measured. The correction factor is the inverse of the amount of time you had the counter gated open for counting (CF = 1 ÷ Gate Time).

For example, if you count a 10 Hz signal for 1 second, your count would be 10. This is multiplied by a correction factor of 1, which is 1 ÷ 1 second. If you count the same 10 Hz signal for 0.5 seconds, your count would be 5. This is multiplied by a correction factor of 2 (1 ÷ 0.5 seconds) which again gives you the true frequency of 10 Hz. Counting 10 Hz for 2 seconds gives you a count of 20 which is then multiplied by a correction factor of 0.5 (1 ÷ 2 seconds) for a result of 10 Hz. In contrast, a more complex example is counting for 131.072 milliseconds (a 16-bit resolution). The correction factor is 1 ÷ .131072, or 7.629.

D/A Conversions

The two D/A converters can be individually programmed to convert 12-bit digital words into a voltage in the range of ±5, ±10, 0 to +5, or 0 to +10 volts. DAC1 is programmed by writing the 12-bit digital data word to BA + 8 and BA + 9. DAC2 is identical, with the data word written to BA + 10 and BA + 11. The DACs are updated by writing to BA + 22. The following tables list the key digital codes and corresponding output voltages for the D/A converters.

D/A Converter Unipolar Calibration Table

D/A Bit Weight	Ideal Output Voltage (in millivolts)	
	0 to +5 V	0 to +10 V
4095 (Max. Output)	4998.8	9997.6
2048	2500.0	5000.0
1024	1250.0	2500.0
512	625.00	1250.0
256	312.50	625.00
128	156.250	312.50
64	78.125	156.250
32	39.063	78.125
16	19.5313	39.063
8	9.7656	19.5313
4	4.8828	9.7656
2	2.4414	4.8828
1	1.2207	2.4414
0	0.0000	0.0000

D/A Converter Bipolar Calibration Table		
	Ideal Output Voltage (in millivolts)	
D/A Bit Weight	±5 V	±10 V
4095 (Max. Output)	+4997.6	+9995.1
2048	0.0	0.0
1024	-2500.0	-5000.0
512	-3750.0	-7500.0
256	-4375.0	-8750.0
128	-4687.5	-9375.0
64	-4843.8	-9687.5
32	-4921.9	-9843.8
16	-4960.9	-9921.9
8	-4980.5	-9960.9
4	-4990.2	-9980.5
2	-4995.1	-9990.2
1	-4997.6	-9995.1
0	-5000.0	-10000.0

User-Available 8254 Timer/Counter

An 8254 programmable interval timer provides three 16-bit, 8 MHz timer/counters for timing and counting functions such as frequency measurement, event counting, and interrupts. All three timer/counters are available for your use. Figure 4-6 shows the timer/counter circuitry.

Each timer/counter has two inputs, CLK in and GATE in, and one output, timer/counter OUT. They can be programmed as binary or BCD down counters by writing the appropriate data to the command word, as described in the I/O map section at the beginning of this chapter.

One of three clock sources, the on-board 2 MHz crystal, external clock 1 (EXT CLK1, P2-41), or external clock 2 (EXT CLK2, P2-45) can be selected as the clock input. The diagram shows how these clock sources are connected to the timer/counters.

Three gate sources are available: +5V on-board (always tied high), external gate 1 (EXT GATE1, P2-42), or external gate 2 (EXT GATE2, P2-46). The diagram shows how these gate sources are connected to the timer/counters.

The output from timer/counter 0 or 1 is jumper-selectable. The selected output is available at the OUT0/OUT1 pin (P2-44). Timer/counter 2's output is available at the TRIGGER OUT/OUT2 (P2-43) if it is enabled by placing the jumper on P3 across the appropriate pins. The diagram shows how these outputs are connected.

The timer/counters can be programmed to operate in one of six modes, depending on your application. The following paragraphs briefly describe each mode.

Mode 0, Event Counter (Interrupt on Terminal Count). This mode is typically used for event counting. While the timer/counter counts down, the output is low, and when the count is complete, it goes high. The output stays high until a new Mode 0 control word is written to the timer/counter.

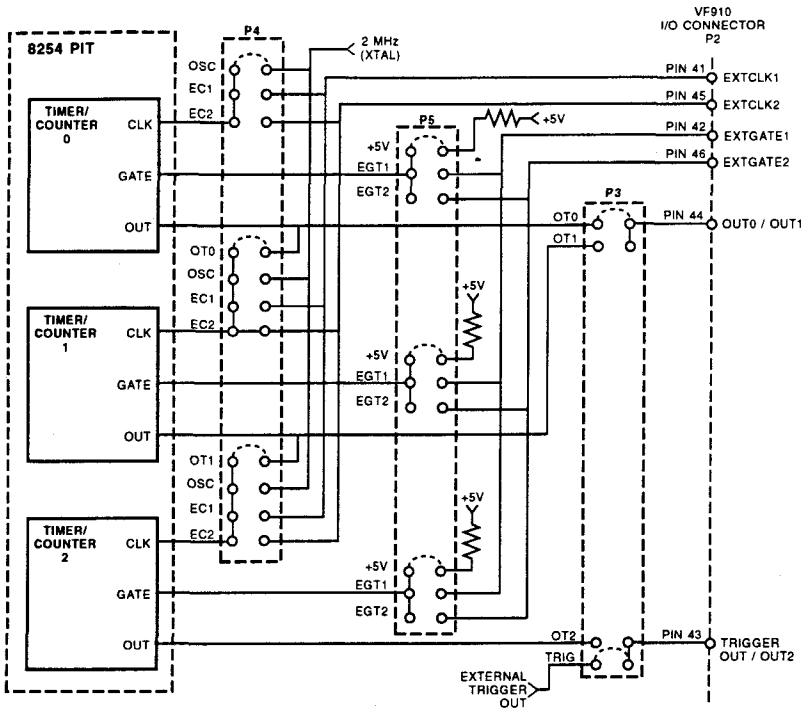


Fig. 4-6 — User 8254 Timer/Counter Circuitry

Mode 1, Hardware-Retriggerable One-Shot. The output is initially high and goes low on the clock pulse following a trigger to begin the one-shot pulse. The output remains low until the count reaches 0, and then goes high and remains high until the clock pulse after the next trigger.

Mode 2, Rate Generator. This mode functions like a divide-by-N counter and is typically used to generate a real-time clock interrupt. The output is initially high, and when the count decrements to 1, the output goes low for one clock pulse. The output then goes high again, the timer/counter reloads the initial count, and the process is repeated. This sequence continues indefinitely.

Mode 3, Square Wave Mode. Similar to Mode 2 except for the duty cycle output, this mode is typically used for baud rate generation. The output is initially high, and when the count decrements to one-half its initial count, the output goes low for the remainder of the count. The timer/counter reloads and the output goes high again. This process repeats indefinitely.

Mode 4, Software-Triggered Strobe. The output is initially high. When the initial count expires, the output goes low for one clock pulse and then goes high again. Counting is "triggered" by writing the initial count.

Mode 5, Hardware Triggered Strobe (Retriggerable). The output is initially high. Counting is triggered by the rising edge of the gate input. When the initial count has expired, the output goes low for one clock pulse and then goes high again.

Digital I/O

The 16 8255 PPI-based digital I/O lines can be used to transfer data between the computer and external devices. The digital input lines can have pull-up or pull-down resistors installed, as described in Chapter 1.

Interrupts

The VF910 has two software selectable interrupt sources: End-of-convert and external trigger. The selected interrupt can be monitored through a software-selectable interrupt channel, IRQ2 through IRQ7. The EOC line is low whenever an A/D conversion is in progress. When the signal transitions to a high (logic 1) state, an interrupt is sent to the computer telling it that the conversion is completed. The external trigger line generates an interrupt on the rising edge or falling edge of the signal fed into P2-39, depending on the setting of bit 1 at BA + 21.

Example Programs

Included with the VF910 is a set of example programs that demonstrate the use of many of the board's features. These examples are in written in C, Pascal, and BASIC. Also included is an easy-to-use menu-driven diagnostics program, 910DIAG, which is especially helpful when you are first checking out your board after installation and when calibrating the board (Chapter 6).

Before using the software included with your board, make a backup copy of the disk. You may make as many backups as you need.

C and Pascal Programs

These programs are source code files so that you can easily develop your own custom software for your VF910 board. In the C directory, VF910.H and VF910.INC contain all of the functions needed to implement the main C programs. H defines the addresses and INC contains the routines called by the main programs. In the Pascal directory, VF910.INC contains all of the procedures needed to implement the main Pascal programs.

Analog-to-Digital:

READ	Demonstrates basic operation of A/D.
EXTTRIG	Similar to READ except that an external trigger is used.
INTRPT, MULTI	Single and multiple channel A/D conversions with interrupt

Digital I/O:

DIGITAL	Simple program the shows how to read and write the digital I/O lines.

Digital-to-Analog:

DAC	Shows how to use the DAC. Uses A/D channel 1 to monitor the output of the DAC.

Interrupts:

INTRPT	Shows the bare essentials required for using interrupts.

BASIC Programs

These programs are source code files so that you can you can easily develop your own custom software for your VF910 board.

Analog-to-Digital:

READ	Demonstrates basic operation of A/D.
EXTTRIG	Similar to READ except that an external trigger is used.

Digital I/O:

DIGITAL	Simple program the shows how to read and write the digital I/O lines.

Digital-to-Analog:

DAC	Shows how to use the DAC. Uses A/D channel 1 to monitor the output of DAC.

CHAPTER 5

CALCULATING FREQUENCIES, VOLTAGES, AND BITS

This chapter contains tables, formulas, and examples to help you understand the principles of V/F conversion. Included are examples which show how to calculate the timer (binary and decimal) to gate the frequency counters and how to calculate the correction factor, tables showing the expected output frequencies for selected input voltages for each input range, and formulas for converting frequency to voltage and bits.

This chapter shows you how to calculate the contents of the 8254 timer which gates the 20-bit A/D conversion counter in both binary (bit-based resolution) and decimal (voltage-based resolution), how to calculate the true frequency of a conversion using the correction factor, expected frequency outputs for selected input voltages for each of the four analog input ranges, and how to convert frequency to voltage and bit values.

Calculating the Settings for the 8254 Timer

When performing voltage-to-frequency conversions, the resolution of your result is dependent on how long you look at the output of the converter. On the VF910, a software selectable system clock drives the V/F converter. The converter divides this clock by 2 internally. Therefore, the output from the V/F converter will always be between 0 and the system clock ÷ 2 (full scale). Using the 20-bit conversion counter, you look at the output of the V/F converter for a specified period of time and count the number of transitions which occur in the output during that time frame. You can set your time period for binary or decimal, depending on whether you want to measure your resolution as a function of bits or voltage.

How long do you want to look at the current conversion before starting a new one? The window of time is set by two 16-bit timers on the 8254 PIT. These timers are cascaded to form a 32-bit timer which is programmed to open up the conversion counter so that you can obtain data at the accuracy level you need for your application.

Binary Calculations

To determine the binary value to be loaded into the timer for bit-based resolutions, you must first calculate what change in the output frequency of the V/F converter you must detect in order to achieve your desired resolution. Note that the input voltage range is not a factor in bit-based calculations. Then, you must divide the system clock which drives the 8254 (the same clock which drives the V/F converter) down to the value of this change in frequency. The result is the value you load into the timer. For example, let's set up the timer for 16-bit conversions.

Calculate the amount of change you must discern for 16 bits:

2^{16} = 65,536, which means you must detect a 1 part change in 65,536 to have a resolution of 16 bits.

Next, convert this result into frequency (0.5 MHz = full scale with a 1 MHz system clock):

500,000 Hz ÷ 65,536 = 7.629394 Hz

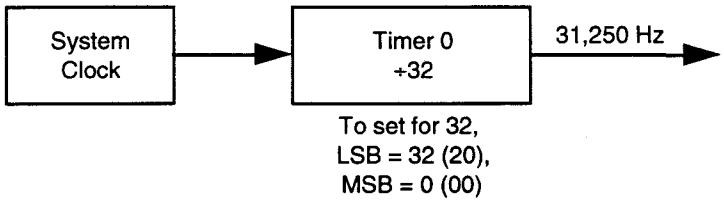
This means that we must detect a change of 7.629394 Hz out of 0.5 MHz. Also note that this frequency, 7.629394 Hz, is the correction factor (see discussion in *Conversion Results and Correction Factor* section).

Next, we must divide the system clock which drives the 8254 by the change we must detect to determine the value we must program into the timer:

1,000,000 ÷ 7.62394 = 1,000,000 ÷ (500,000 ÷ 65,536) = 2 x 65,536 = 131,072

We need to divide the system clock by 131,072 to open the timer for the right amount of time, 131.072 milliseconds, to take 16-bit readings.

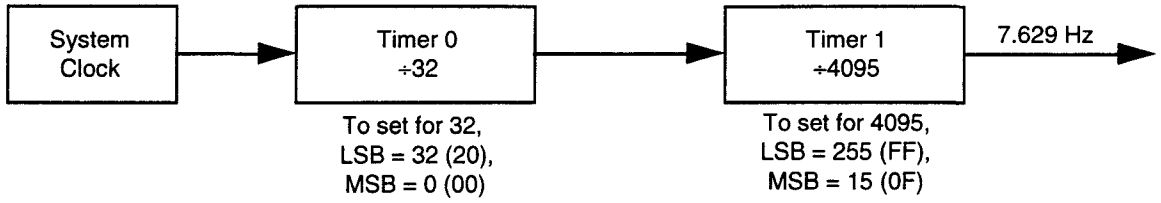
Counter 0 is programmed with the 16 least significant bits of the 32-bit timer word. All of our example programs use binary division and set counter 0 to 32. When counter 0 is 32, the 1 MHz clock is divided by 32 for a resulting 31,250 Hz clock into timer 1, as shown below:



Then, timer 1, which contains the 16 most significant bits of the 32-bit timer word, is programmed. The value to be programmed is determined by:

(131,072 ÷ 32) - 1 = 4095

The value we must program in timer 1 is 4095, as shown in the diagram below.



The values calculated using the formulas already presented will open the window of the counters for the right amount of time whenever you are doing conversions. Note that you always subtract 1 from the timer value in order to correct for the 8254's method of loading and counting. The table below shows the count which must be loaded into the timers for the listed bit-based resolutions for *Single Convert* and for *Continuous Convert* modes.

Resolution	Timer 0 LSB (Decimal/Hex)	Timer 0 MSB (Decimal/Hex)	Timer 1 LSB (Decimal/Hex)	Timer 1 MSB (Decimal/Hex)
12 bits	32 / 20	0 / 00	255 / FF	0 / 00
13 bits	32 / 20	0 / 00	255 / FF	1 / 01
14 bits	32 / 20	0 / 00	255 / FF	3 / 03
15 bits	32 / 20	0 / 00	255 / FF	7 / 07
16 bits	32 / 20	0 / 00	255 / FF	15 / 0F
17 bits	32 / 20	0 / 00	255 / FF	31 / 1F
18 bits	32 / 20	0 / 00	255 / FF	63 / 3F

Decimal Calculations

To determine the decimal value to be loaded into the timer for voltage-based resolutions, you must first calculate what change in the output frequency of the V/F converter you must detect in order to achieve your desired resolution. Unlike with the bit-based formulas, you must include the input voltage range in this calculation. Then, you must divide the system clock which drives the 8254 (the same clock which drives the V/F converter) down to the value of this change in frequency. The result is the value you load into the timer. For example, let's set up the timer for conversions with a resolution of 100 microvolts.

Calculate the amount of change you must discern for 100 microvolt resolution and an input range of 10 volts:

5 V ÷ 100 μV = 50,000, which means you must detect a 1 part change in 50,000 to have a resolution of 100 microvolts.

Next, convert this result into frequency (0.5 MHz = full scale for a 1 MHz system clock):

500,000 Hz ÷ 50,000 = 10 Hz

This means that we must detect a change of 10 Hz out of 0.5 MHz. Also note that this frequency, 10 Hz, is the correction factor (see discussion in *Conversion Results and Correction Factor* section).

Next, we must divide the system clock which drives the 8254 by the change we must detect to determine the value we must program into the timer:

1,000,000 ÷ 10 = 100,000

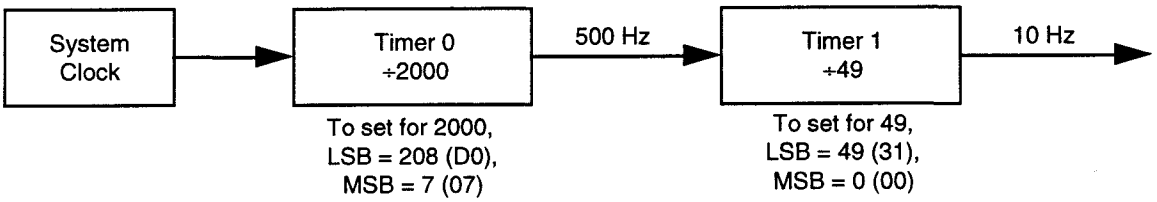
We need to divide the 1 MHz clock by 100,000 to open the timer for the right amount of time, 100 milliseconds, to take 100 microvolt resolution readings.

Counter 0 is programmed with the 16 least significant bits of the 32-bit timer word. When counter 0 is 2000, the 1 MHz clock is divided by 2000 for a resulting 0.5 kHz clock into timer 1.

Then, timer 1, which contains the 16 most significant bits of the 32-bit timer word, is programmed. The value to be programmed is determined by:

(100,000 ÷ 2000) - 1 = 49

The value we must program in timer 1 is 49, as shown in the diagram below.



Like in binary calculations, the values calculated using the formulas already presented will open the window of the counters for the right amount of time whenever you are doing conversions. Note that you always subtract 1 from the timer value in order to correct for the 8254's method of loading and counting. The two tables on the following page show the count which must be loaded into the timers for input ranges of 5 volts or 10 volts for the listed voltage-based resolutions.

For 5-volt Input Ranges:				
Resolution	**Timer 0 LSB (Decimal/Hex)**	**Timer 0 MSB (Decimal/Hex)**	**Timer 1 LSB (Decimal/Hex)**	**Timer 1 MSB (Decimal/Hex)**
10 mV	250 / FA	0 / 00	3 / 03	0 / 00
1 mV	208 / D0	7 / 07	4 / 04	0 / 00
100 µV	208 / D0	7 / 07	49 / 31	0 / 00
10 µV	208 / D0	7 / 07	243 / F3	1 / 01

For 10-volt Input Ranges:				
Resolution	**Timer 0 LSB (Decimal/Hex)**	**Timer 0 MSB (Decimal/Hex)**	**Timer 1 LSB (Decimal/Hex)**	**Timer 1 MSB (Decimal/Hex)**
10 mV	244 / F4	1 / 01	3 / 03	0 / 00
1 mV	208 / D0	7 / 07	9 / 09	0 / 00
100 µV	208 / D0	7 / 07	99 / 63	0 / 00
10 µV	208 / D0	7 / 07	231 / E7	3 / 03

Conversion Results and Correction Factor

For each conversion, when you count the output of the V/F converter, you increment a 20-bit counter by one for each pulse counted. For example, let's program the timer to open the gate for the counter for a period of 131.072 milliseconds. We read the data from the counter in three 8-bit words, ADLB (low byte), ADMB (middle byte), and ADHB (high byte). To find the true frequency represented by the count, you calculate:

True Frequency = [(ADLB + (ADMB x 256) + (ADHB x 65536)] x CF

where CF is the correction factor.

After performing the multiplication by the bit weight for each of the three bytes read, you must then multiply the result by CF, the correction factor, in order to find the true frequency of the signal you measured. The correction factor is the inverse of the amount of time you had the counter gated open for counting:

CF = 1/Gate Time

For example, if you count a 10 Hz signal for 1 second, your count would be 10. This is multiplied by a correction factor of 1, which is the same as 1 ÷ 1 second. If you count the same 10 Hz signal for 0.5 seconds, your count would be 5. This is multiplied by a correction factor of 2 (1 ÷ 0.5 seconds) which again gives you the true frequency of 10 Hz. Counting 10 Hz for 2 seconds gives you a count of 20 which is then multiplied by a correction factor of 0.5 (1 ÷ 2 seconds) for a result of 10 Hz. In contrast, a more complex example is counting for 131.072 milliseconds (our 16-bit resolution example given above). The correction factor is 1 ÷ 0.131072, or 7.629.

The upper four bits of the high byte (ADHB) contain the measurement overflow, counter overflow, and conversion done flags. These flags must be masked out when you calculate the frequency or voltage value.

Input Voltages and Output Frequencies

The analog inputs can be set up for four ranges: 0 to +5, 0 to +10, -2.5 to +2.5, and -5 to +5 volts. The following tables show the expected output frequencies for selected input voltages in each range for a 1 MHz system clock.

For 0 to +5V range: (Frequency = 100,000 x Input Voltage)	
Input Voltage	**Output Frequency**
5V	500,000 Hz
3.75V	375,000 Hz
2.5V	250,000 Hz
1.25V	125,000 Hz
0V	0 Hz

For 0 to +10V range: (Frequency = 50,000 x Input Voltage)	
Input Voltage	**Output Frequency**
10V	500,000 Hz
7.5V	375,000 Hz
5V	250,000 Hz
2.5V	125,000 Hz
0V	0 Hz

For -2.5 to +2.5V range: (Frequency = 100,000 x (Input Voltage + 2.5))	
Input Voltage	**Output Frequency**
+2.5V	500,000 Hz
+1.25V	375,000 Hz
0V	250,000 Hz
-1.25V	125,000 Hz
-2.5V	0 Hz

For -5 to +5V range: (Frequency = 50,000 x (Input Voltage + 5))	
Input Voltage	**Output Frequency**
+5V	500,000 Hz
+2.5V	375,000 Hz
0V	250,000 Hz
-2.5V	125,000 Hz
-5V	0 Hz

Input Voltage Calculations

The general formula for calculating the input voltage when the frequency and voltage range are known is:

Input Voltage = (Frequency/(system clock ÷ 2/Voltage Range) - Offset

The offset is 0 for unipolar voltage ranges and one-half the range for bipolar voltage ranges.

For 0 to +5 volts:

Input Voltage = (Frequency/100,000) - 0

For 0 to +10 volts:

Input Voltage = (Frequency/50,000) - 0

For -2.5 to +2.5 volts:

Input Voltage = (Frequency/100,000) - 2.5

For -5 to +5 volts:

Input Voltage = (Frequency/50,000) - 5

Bit Calculations

The general formula for calculating the bit value when the frequency and resolution are known is:

Bit Value = (Frequency/(system clock ÷ $2/2^N$)) - Offset

where N = the number of bits of the desired resolution,
and the offset is 0 for unipolar operation and 0.5×2^N for bipolar operation.

For example, to calculate the bit value for a 12-bit resolution:

Unipolar: Bit Value = (Frequency/(system clock ÷ 2/4096)) - 0
= Frequency/122.07

Bipolar: Bit Value = (Frequency/(system clock ÷ 2/4096)) - 2048
= (Frequency/122.07) - 2048

For example, to calculate the bit value for a 16-bit resolution:

Unipolar: Bit Value = (Frequency/(system clock ÷ 2/65,536)) - 0
= Frequency/7.629

Bipolar: Bit Value = (Frequency/(system clock ÷ 2/65,536)) - 32,768
= (Frequency/7.629) - 32,768

CHAPTER 6

CALIBRATION

This chapter tells you how to calibrate the VF910 using the 910DIAG diagnostics program included in the example software package and the four trimpots on the board. These trimpots calibrate the V/F converter gain and offset and the D/A circuitry. Calibration is necessary whenever you change the analog input voltage range and/or polarity.

This chapter tells you how to calibrate the V/F converter gain and offset and the D/A converter X2 multiplier. The offset and full-scale performance of the board's V/F converter is factory-calibrated for operation at the input voltage range you specified when ordering the board. If you change the range and/or polarity, you must recalibrate your board. Any time you suspect inaccurate readings, you can check the accuracy of your conversions using the procedure below, and make adjustments as necessary.

Calibration is done with the board installed in your PC. You can access the trimpots with the computer's cover removed. Power up the computer and let the board circuitry stabilize for 15 minutes before you start calibrating.

Required Equipment

The following equipment is required for calibration:

- 910DIAG Diagnostics Program (included with example software)
- Precision Voltage Source: ±10 volts
- Digital Voltmeter: 5-1/2 digits
- Small Screwdriver (for trimpot adjustment)

Figure 6-1 shows the board layout. The four trimpots used for calibration, TR1, TR2, TR4, and TR5, are located in the upper center area of the board.

V/F Calibration

Two adjustments are made to calibrate the V/F converter. One is the offset adjustment, and the other is the full scale, or gain, adjustment. Trimpot TR2 is used to make the offset adjustment, and trimpot TR1 is used for gain adjustment.

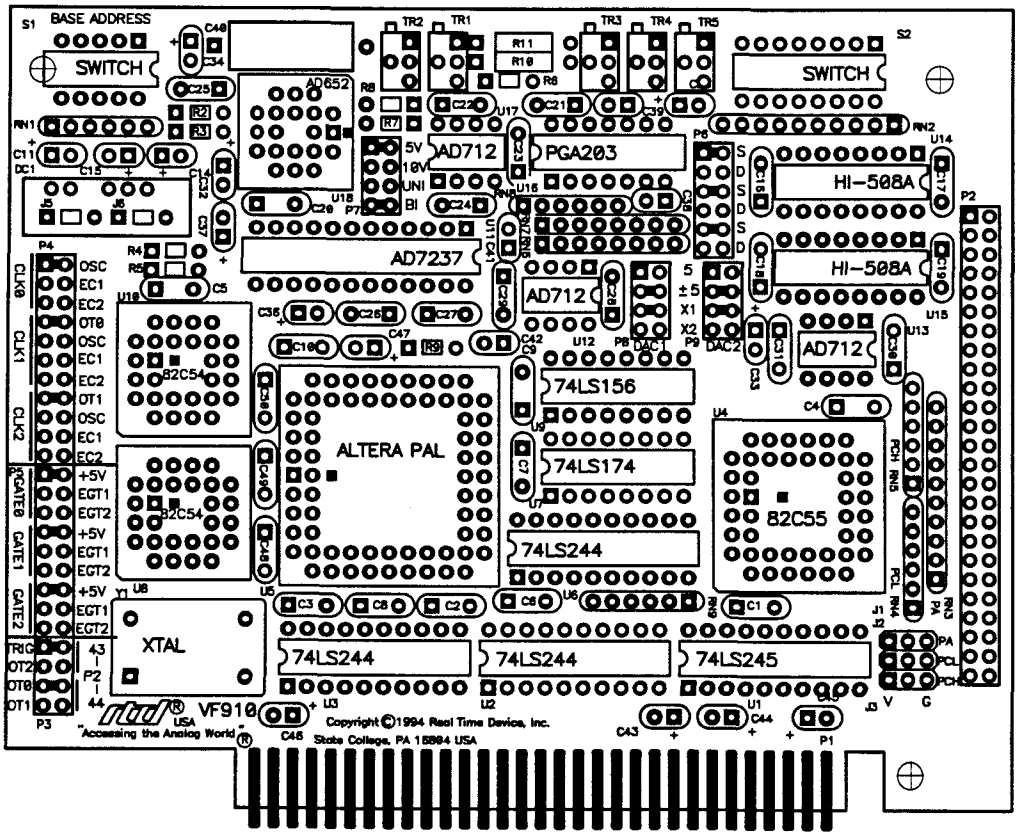


Fig. 6-1 — Board Layout

Connect your voltage source to channel 1 on the VF910 board. Use Table 6-1 to set the voltage for your input range and desired adjustment (offset or gain). Then run the 910DIAG program, adjusting the appropriate trimpot until the input voltage and V/F converter output reading match.

Table 6-1 — A/D Offset and Gain Adjustments

Input Voltage	TR1, Gain	TR2, Offset
0 to +5 volt input range:		
.0001 V	—	.0001 V
+4.75 V	+4.75 V	—
0 to +10 volt input range:		
.0001 V	—	.0001 V
+9.75 V	+9.75 V	—
-2.5 to +2.5 volt input range:		
0 V	—	0 V
+2.25 V	+2.25 V	—
-5 to +5 volt input range:		
0 V	—	0 V
+4.75 V	+4.75 V	—

D/A Calibration

The D/A converter requires no calibration for the X1 ranges (0 to +5 and ±5 volts). The following paragraph describes the calibration procedure for the X2 multiplier ranges.

To calibrate for X2 (0 to +10 or ±10 volts), set the DAC output voltage range to 0 to +10 volts (jumpers on X2 and 5 on P6, AOUT1, or P7, AOUT2). Then, program the corresponding D/A converter (DAC1 or DAC2) with the digital value 2048. The ideal DAC output for 2048 at X2 (0 to +10 volt range) is 5.0000 volts. Adjust TR4 for AOUT1 and TR5 for AOUT2 until 5.0000 volts is read at the output. Table 6-2 lists the ideal output voltages per bit weight for unipolar ranges and Table 6-3 lists the ideal output voltages for bipolar ranges.

Table 6-2 — D/A Converter Unipolar Calibration Table		
	Ideal Output Voltage (in millivolts)	
D/A Bit Weight	0 to +5 V	0 to +10 V
4095 (Max. Output)	4998.8	9997.6
2048	2500.0	5000.0
1024	1250.0	2500.0
512	625.00	1250.0
256	312.50	625.00
128	156.250	312.50
64	78.125	156.250
32	39.063	78.125
16	19.5313	39.063
8	9.7656	19.5313
4	4.8828	9.7656
2	2.4414	4.8828
1	1.2207	2.4414
0	0.0000	0.0000

Table 6-3 — D/A Converter Bipolar Calibration Table		
	Ideal Output Voltage (in millivolts)	
D/A Bit Weight	±5 V	±10 V
4095 (Max. Output)	+4997.6	+9995.1
2048	0.0	0.0
1024	-2500.0	-5000.0
512	-3750.0	-7500.0
256	-4375.0	-8750.0
128	-4687.5	-9375.0
64	-4843.8	-9687.5
32	-4921.9	-9843.8
16	-4960.9	-9921.9
8	-4980.5	-9960.9
4	-4990.2	-9980.5
2	-4995.1	-9990.2
1	-4997.6	-9995.1
0	-5000.0	-10000.0

APPENDIX A

VF910 SPECIFICATIONS

VF910 Characteristics Typical @ 25° C

Interface

IBM PC/XT/AT compatible
Switch-selectable base address, I/O mapped
Software-selectable interrupt

Analog Input

8 differential, 8 single-ended with dedicated ground, 16 single-ended
Input impedance, each channel ..... >10 megohms
Input ranges ..... 0 to +5, 0 to +10, ±2.5, or ±5 volts
Overvoltage protection ..... ±35 Vdc
Gains, software selectable ..... 1, 2, 4 & 8 plus Gm gain multiplier
Gain error ..... 0.05%, typ; 0.25%, max
Common mode input voltage ..... ±10 volts, max
Settling time (gain = 1) ..... 10 µsec, max

V/F Converter AD652

Type ..... Synchronous
Resolution ..... to 18 bits (19 µV, 5-volt range)
Linearity error ..... 0.005%, max
Conversion speed ..... See table below

Digital I/O ..... CMOS 82C55

Number of lines 16
Logic compatibility ..... TTL/CMOS
(Configurable with optional I/O pull-up/pull-down resistors)
High-level output voltage ..... 4.2V, min
Low-level output voltage ..... 0.45V, max
High-level input voltage ..... 2.2V, min; 5.5V, max
Low-level input voltage ..... -0.3V, min; 0.8V, max
Input load current ..... ±10 µA
Input capacitance,
C(IN)@F=1MHz ..... 10 pF
Output capacitance,
C(OUT)<@F=1MHz ..... 20 pF

D/A Converter AD7237

Analog outputs ..... 2 channels
Resolution ..... 12 bits
Output ranges ..... 0 to +5, ±5, or 0 to +10 volts
Guaranteed linearity across output ranges ..... 0 to +5, ±5, and 0 to +9.2 volts
Relative accuracy ..... ±1 LSB, max
Full-scale accuracy ..... ±5 LSB, max
Non-linearity ..... ±1 LSB, max
Settling time ..... 10 µsec, max

Timer/Counters ..... CMOS 82C54

Three 16-bit down counters (2 cascaded, 1 independent)
6 programmable operating modes
Counter input source ..... External clock (8 MHz, max) or on-board 2 MHz clock
Counter outputs ..... Available externally
Counter gate source ..... External gate or always enabled

Miscellaneous Inputs/Outputs (PC bus-sourced)

+5 volts, ±12 volts, ground

Current Requirements

520 mA @ +5 volts

Connector

50-pin right angle shrouded box header

Environmental

Operating temperature ..... 0 to +70°C
Storage temperature ..... -40 to +85°C
Humidity ..... 0 to 90% non-condensing

Size

Short slot — 3.875"H x 5.30"W (99mm x 135mm)

VF910 A/D Conversion Resolution (1 MHz System Clock)

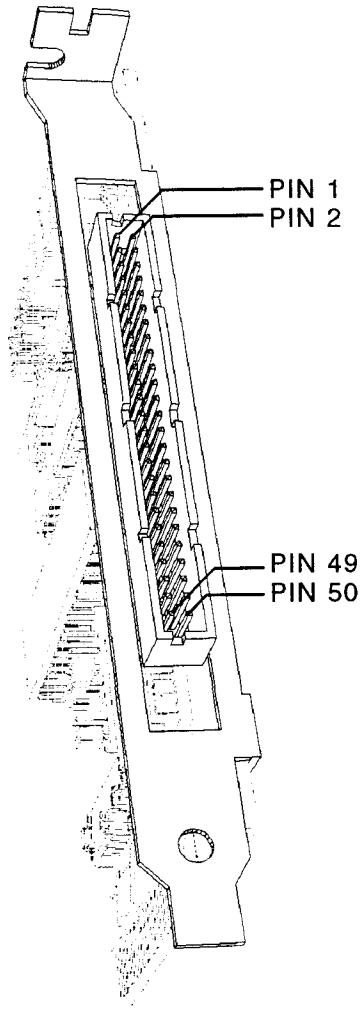
RESOLUTION	CONVERSION TIME	FREQUENCY
10 bits	2.048 msec	488.28 Hz
11 bits	4.096 msec	244.14 Hz
12 bits	8.192 msec	122.07 Hz
13 bits	16.384 msec	61.04 Hz
14 bits	32.768 msec	30.52 Hz
15 bits	65.536 msec	15.26 Hz
16 bits	131.072 msec	7.63 Hz
17 bits	262.144 msec	3.81 Hz
18 bits	524.288 msec	1.90 Hz

APPENDIX B

P2 CONNECTOR PIN ASSIGNMENTS

P2 Connector:

DIFF.	S.E.			DIFF.	S.E.
AIN1+	AIN1	1	2	AIN1-	AIN9 / AGND
AIN2+	AIN2	3	4	AIN2-	AIN10 / AGND
AIN3+	AIN3	5	6	AIN3-	AIN11 / AGND
AIN4+	AIN4	7	8	AIN4-	AIN12 / AGND
AIN4+	AIN5	9	10	AIN5-	AIN13 / AGND
AIN6+	AIN6	11	12	AIN6-	AIN14 / AGND
AIN7+	AIN7	13	14	AIN7-	AIN15 / AGND
AIN8+	AIN8	15	16	AIN8-	AIN16 / AGND
	AOUT 1	17	18	ANALOG GND	
	AOUT 2	19	20	ANALOG GND	
	ANALOG GND	21	22	ANALOG GND	
	PA7	23	24	PC7	
	PA6	25	26	PC6	
	PA5	27	28	PC5	
	PA4	29	30	PC4	
	PA3	31	32	PC3	
	PA2	33	34	PC2	
	PA1	35	36	PC1	
	PA0	37	38	PC0	
	TRIGGER IN	39	40	DIGITAL GND	
	EXT CLK1	41	42	EXT GATE1	
	TRIGGER OUT / OUT2	43	44	OUT0 / OUT1	
	EXT CLK2	45	46	EXT GATE2	
	+12 VOLTS	47	48	+5 VOLTS	
	-12 VOLTS	49	50	DIGITAL GND	



Mating Connector Part Numbers	
Manufacturer	**Part Number**
AMP	1-746094-0
3M	3425-7650

APPENDIX C

COMPONENT DATA SHEETS

Intel 82C54 Programmable Interval Timer
Data Sheet Reprint

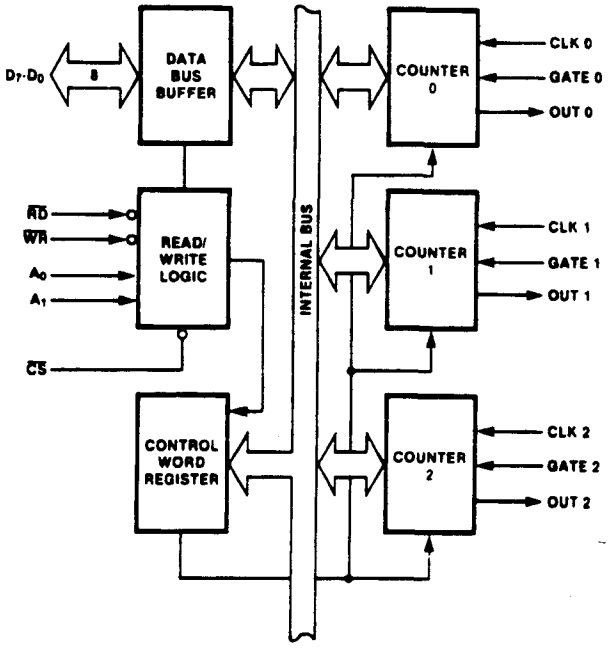
82C54
CHMOS PROGRAMMABLE INTERVAL TIMER

- **Compatible with all Intel and most other microprocessors**
- **High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188**
- **Handles Inputs from DC to 8 MHz — 10 MHz for 82C54-2**
- **Available in EXPRESS**
  - **Standard Temperature Range**
  - **Extended Temperature Range**
- **Three independent 16-bit counters**
- **Low Power CHMOS**
  - **I_{CC} = 10 mA @ 8 MHz Count frequency**
- **Completely TTL Compatible**
- **Six Programmable Counter Modes**
- **Binary or BCD counting**
- **Status Read Back Command**
- **Available in 24-Pin DIP and 28-Pin PLCC**

The Intel 82C54 is a high-performance, CHMOS version of the industry standard 8254 counter/timer which is designed to solve the timing control problems common in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 82C54 is pin compatible with the HMOS 8254, and is a superset of the 8253.

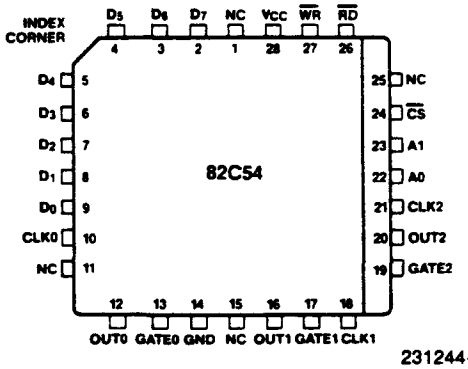
Six programmable timer modes allow the 82C54 to be used as an *event counter*, *elapsed time indicator*, programmable one-shot, and in many other applications.

The 82C54 is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent HMOS product. The 82C54 is available in 24-pin DIP and 28-pin plastic leaded chip carrier (PLCC) packages.



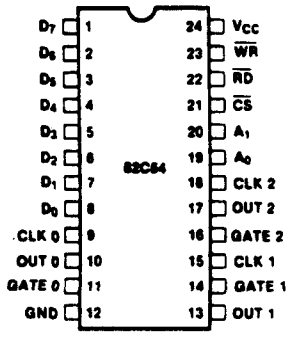
231244-1

Figure 1. 82C54 Block Diagram



231244-3

PLASTIC LEADED CHIP CARRIER



231244-2

Diagrams are for pin reference only.
Package sizes are not to scale.

Figure 2. 82C54 Pinout

September 1989
Order Number: 231244-005

Table 1. Pin Description

Symbol	Pin Number		Type	Function
	DIP	PLCC		
D_7-D_0	1-8	2-9	I/O	Data: Bidirectional tri-state data bus lines, connected to system data bus.
CLK 0	9	10	I	Clock 0: Clock input of Counter 0.
OUT 0	10	12	O	Output 0: Output of Counter 0.
GATE 0	11	13	I	Gate 0: Gate input of Counter 0.
GND	12	14		Ground: Power supply connection.
OUT 1	13	16	O	Out 1: Output of Counter 1.
GATE 1	14	17	I	Gate 1: Gate input of Counter 1.
CLK 1	15	18	I	Clock 1: Clock input of Counter 1.
GATE 2	16	19	I	Gate 2: Gate input of Counter 2.
OUT 2	17	20	O	Out 2: Output of Counter 2.
CLK 2	18	21	I	Clock 2: Clock input of Counter 2.
A_1, A_0	20-19	23-22	I	Address: Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.
				A_1 | A_0 | Selects 0 | 0 | Counter 0 0 | 1 | Counter 1 1 | 0 | Counter 2 1 | 1 | Control Word Register
$\overline{CS}$	21	24	I	Chip Select: A low on this input enables the 82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	26	I	Read Control: This input is low during CPU read operations.
$\overline{WR}$	23	27	I	Write Control: This input is low during CPU write operations.
V_{CC}	24	28		Power: +5V power supply connection.
NC		1, 11, 15, 25		No Connect

FUNCTIONAL DESCRIPTION

General

The 82C54 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other counter/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real time clock
- Even counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Block Diagram

DATA BUS BUFFER

This 3-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus (see Figure 3).

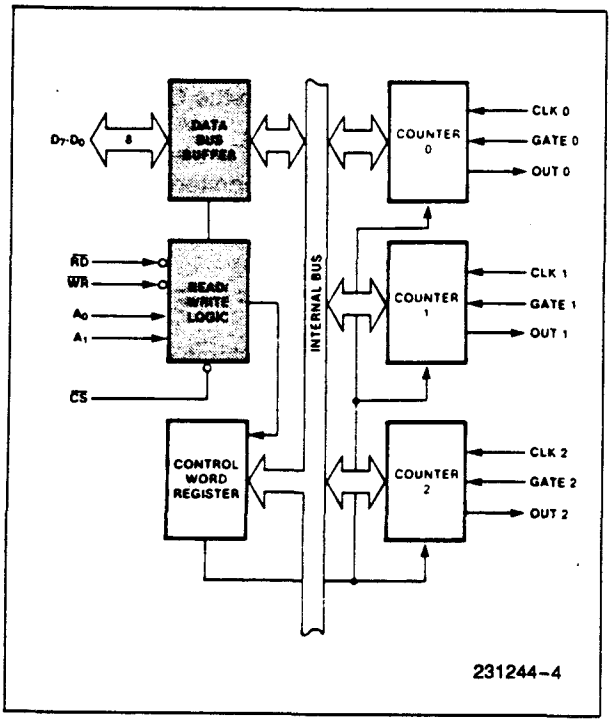


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

READ/WRITE LOGIC

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A_1 and A_0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the 82C54 that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the 82C54 has been selected by holding $\overline{CS}$ low.

CONTROL WORD REGISTER

The Control Word Register (see Figure 4) is selected by the Read/Write Logic when A_1, A_0 = 11. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

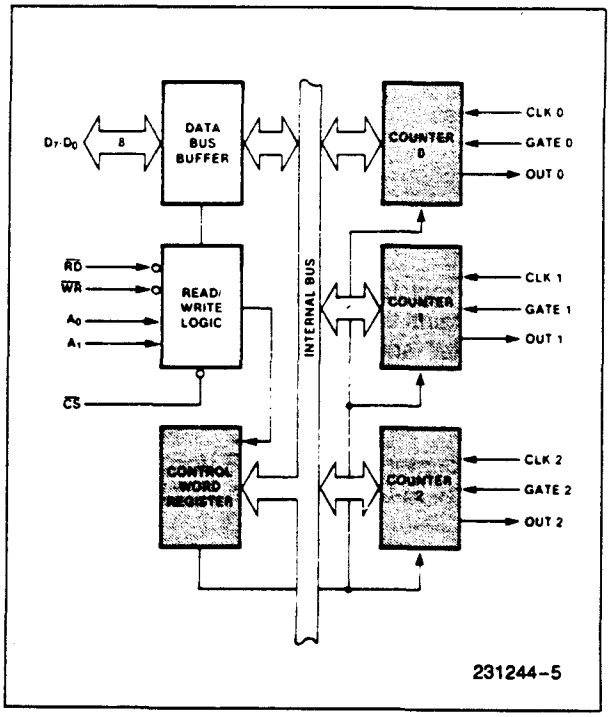


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

COUNTER 0, COUNTER 1, COUNTER 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 5.

The Counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

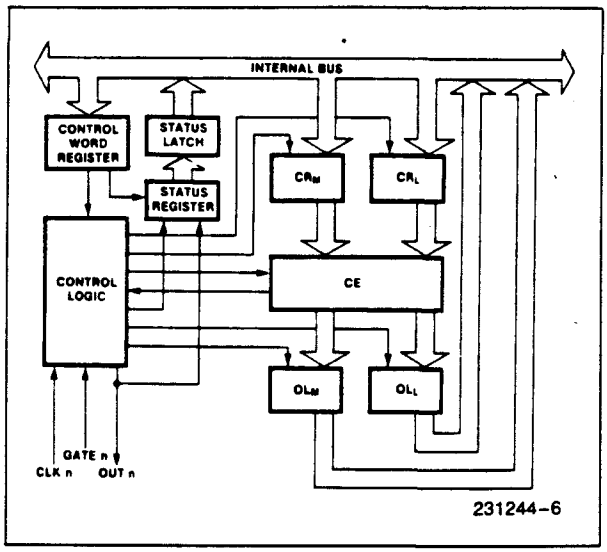


Figure 5. Internal Block Diagram of a Counter

The status register, shown in the Figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labelled CE (for "Counting Element"). It is a 16-bit presettable synchronous down counter.

OL_M and OL_L are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L stand for "Most significant byte" and "Least significant byte" respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CR_M and CR_L (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR_M and CR_L are cleared when the Counter is programmed. In this way, if the Counter has been programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

82C54 SYSTEM INTERFACE

The 82C54 is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A_0, A_1 connect to the A_0, A_1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel 8205 for larger systems.

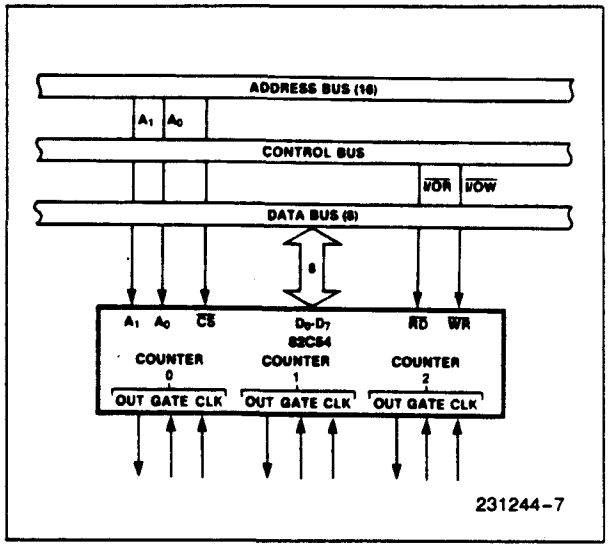


Figure 6. 82C54 System Interface

OPERATIONAL DESCRIPTION

General

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the 82C54

Counters are programmed by writing a Control Word and then an initial count. The control word format is shown in Figure 7.

All Control Words are written into the Control Word Register, which is selected when A_1, A_0 = 11. The Control Word itself specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A_1, A_0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Control Word Format

A_1, A_0 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW — Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

NOTE: Don't care bits (X) should be 0 to insure compatibility with future Intel products.

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Figure 7. Control Word Format

Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

1) For each Counter, the Control Word must be written before the initial count is written.
2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A_1, A_0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

		A_1	A_0
Control Word —	Counter 0	1	1
LSB of count —	Counter 0	0	0
MSB of count —	Counter 0	0	0
Control Word —	Counter 1	1	1
LSB of count —	Counter 1	0	1
MSB of count —	Counter 1	0	1
Control Word —	Counter 2	1	1
LSB of count —	Counter 2	1	0
MSB of count —	Counter 2	1	0

		A_1	A_0
Control Word —	Counter 2	1	1
Control Word —	Counter 1	1	1
Control Word —	Counter 0	1	1
LSB of count —	Counter 2	1	0
MSB of count —	Counter 2	1	0
LSB of count —	Counter 1	0	1
MSB of count —	Counter 1	0	1
LSB of count —	Counter 0	0	0
MSB of count —	Counter 0	0	0

		A_1	A_0
Control Word —	Counter 0	1	1
Counter Word —	Counter 1	1	1
Control Word —	Counter 2	1	1
LSB of count —	Counter 2	1	0
LSB of count —	Counter 1	0	1
LSB of count —	Counter 0	0	0
MSB of count —	Counter 0	0	0
MSB of count —	Counter 1	0	1
MSB of count —	Counter 2	1	0

		A_1	A_0
Control Word —	Counter 1	1	1
Control Word —	Counter 0	1	1
LSB of count —	Counter 1	0	1
Control Word —	Counter 2	1	1
LSB of count —	Counter 0	0	0
MSB of count —	Counter 1	0	1
LSB of count —	Counter 2	1	0
MSB of count —	Counter 0	0	0
MSB of count —	Counter 2	1	0

NOTE:
In all four examples, all counters are programmed to read/write two-byte counts.
These are only four of many possible programming sequences.

Figure 8. A Few Possible Programming Sequences

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 82C54.

There are three possible methods for reading the counters: a simple read operation, the Counter Latch Command, and the Read-Back Command. Each is explained below. The first method is to perform a simple read operation. To read the Counter, which is selected with the A1, A0 inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.

COUNTER LATCH COMMAND

The second method uses the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A_1, A_0 = 11. Also like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

A_1, A_0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5,D4 - 00 designates Counter Latch Command

X - don't care

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 9. Counter Latching Command Format

The selected Counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until it is read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the 82C54 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read/write two-byte counts, the following precaution applies; A program must not transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

READ-BACK COMMAND

The third method uses the Read-Back command. This command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 10. The command applies to the counters selected by setting their corresponding bits D3,D2,D1 = 1.

A0, A1 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D_5: 0 = Latch count of selected counter(s)
D_4: 0 = Latch status of selected counter(s)
D_3: 1 = Select counter 2
D_2: 1 = Select counter 1
D_1: 1 = Select counter 0
D_0: Reserved for future expansion; must be 0

Figure 10. Read-Back Command Format

The read-back command may be used to latch multiple counter output latches (OL) by setting the $\overline{COUNT}$ bit D5 = 0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the

count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting $\overline{\text{STATUS}}$ bit D4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 11. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D_7 1 = Out Pin is 1
0 = Out Pin is 0
D_6 1 = Null count
0 = Count available for reading
D_5-D_0 Counter Programmed Mode (See Figure 7)

Figure 11. Status Byte

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 12.

THIS ACTION:	CAUSES:
A. Write to the control word register:[1]	Null count = 1
B. Write to the count register (CR);[2]	Null count = 1
C. New count is loaded into CE (CR → CE);	Null count = 0

[1] Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.

[2] If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

Figure 12. Null Count Operation

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both $\overline{\text{COUNT}}$ and $\overline{\text{STATUS}}$ bits D5,D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 13.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

Command								Description	Results
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Figure 13. Read-Back Command Example

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Figure 14. Read/Write Operations Summary

Mode Definitions

The following are defined for use in describing the operation of the 82C54.

CLK PULSE: a rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER: a rising edge of a Counter's GATE input.

COUNTER LOADING: the transfer of a count from the CR to the CE (refer to the "Functional Description")

MODE 0: INTERRUPT ON TERMINAL COUNT

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

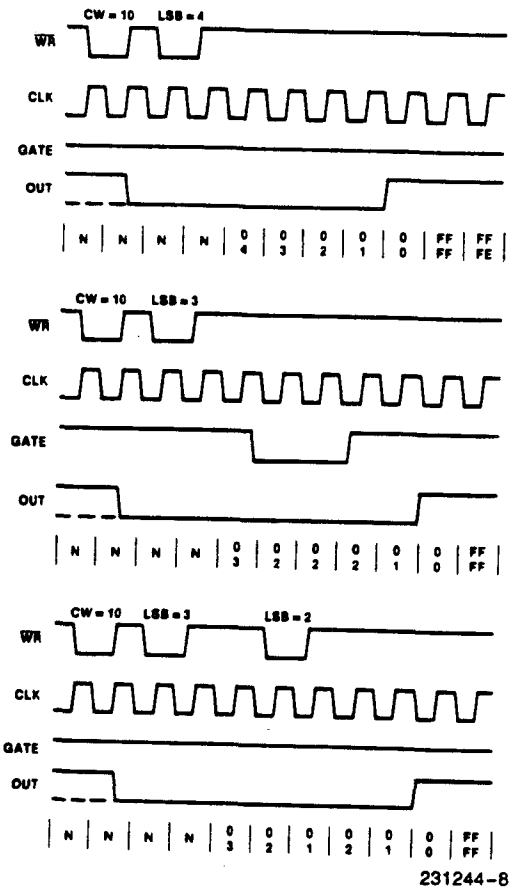
After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.



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NOTE:
The Following Conventions Apply To All Mode Timing Diagrams:
1. Counters are programmed for binary (not BCD) counting and for Reading/Writing least significant byte (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB stands for "Least Significant Byte" of count.
5. Numbers below diagrams are count values.
The lower number is the least significant byte.
The upper number is the most significant byte. Since the counter is programmed to Read/Write LSB only, the most significant byte cannot be read.
N stands for an undefined count.
Vertical lines show transitions between count values.

Figure 15. Mode 0

MODE 1: HARDWARE RETRIGGERABLE ONE-SHOT

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

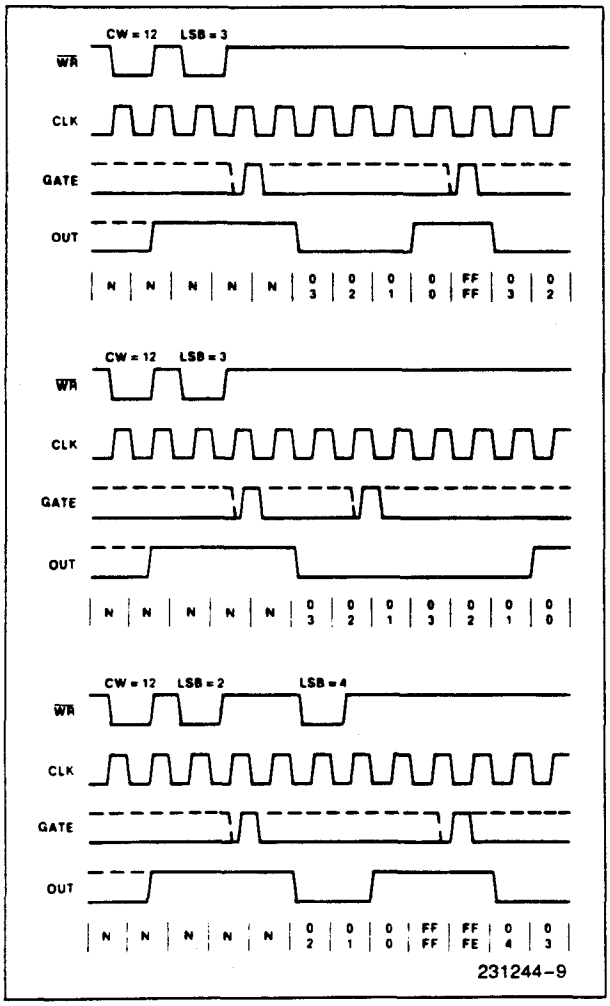


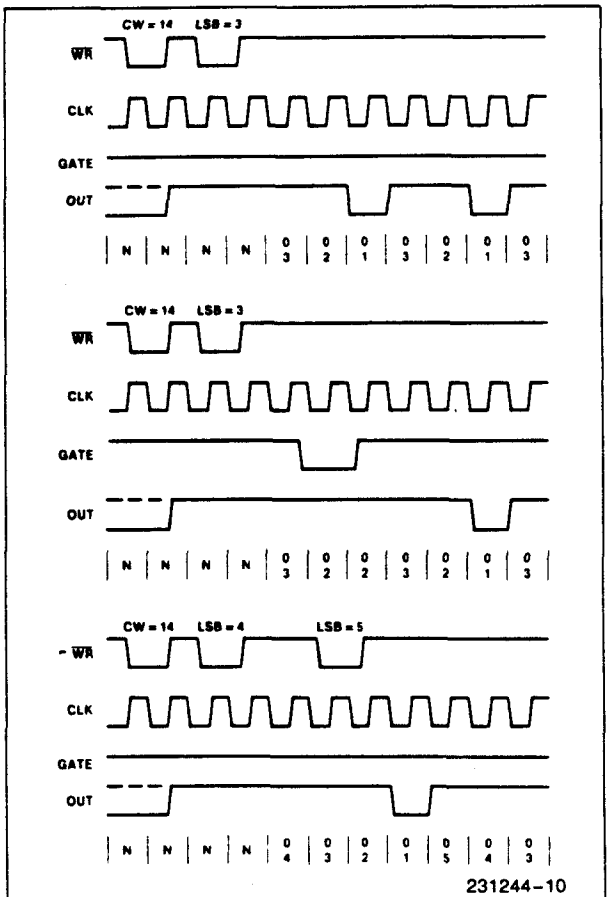
Figure 16. Mode 1

MODE 2: RATE GENERATOR

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.



NOTE:
A GATE transition should not occur one clock prior to terminal count.

Figure 17. Mode 2

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

MODE 3: SQUARE WAVE MODE

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

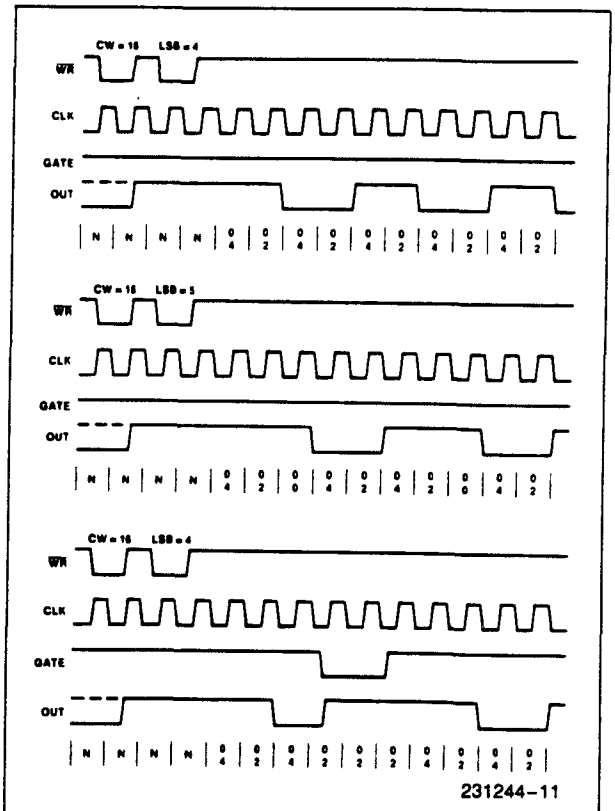
After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse *after* the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N − 1)/2 counts.



NOTE:
A GATE transition should not occur one clock prior to terminal count.

Figure 18. Mode 3

MODE 4: SOFTWARE TRIGGERED STROBE

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N+1 CLK pulses after the new count of N is written.

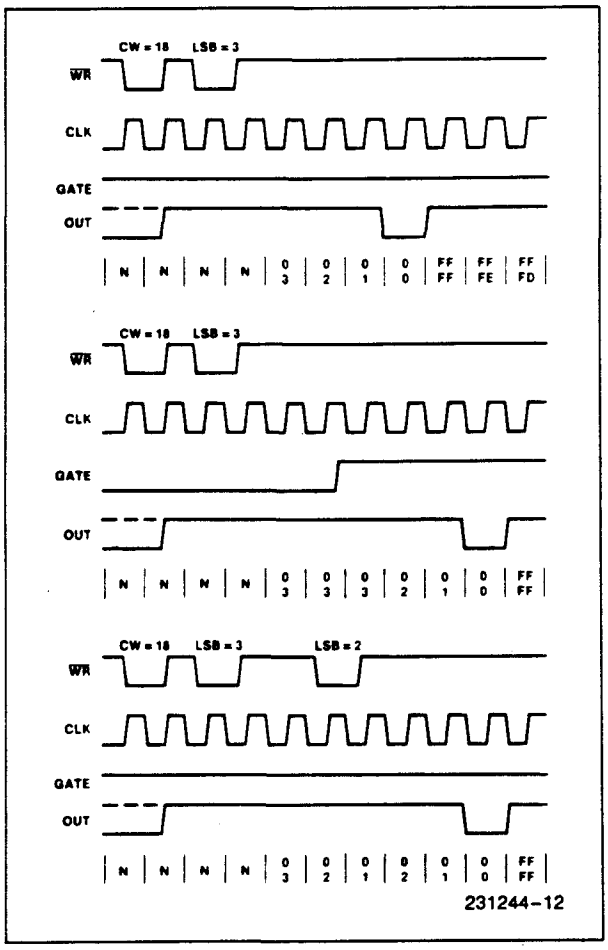


Figure 19. Mode 4

MODE 5: HARDWARE TRIGGERED STROBE (RETRIGGERABLE)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after a trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

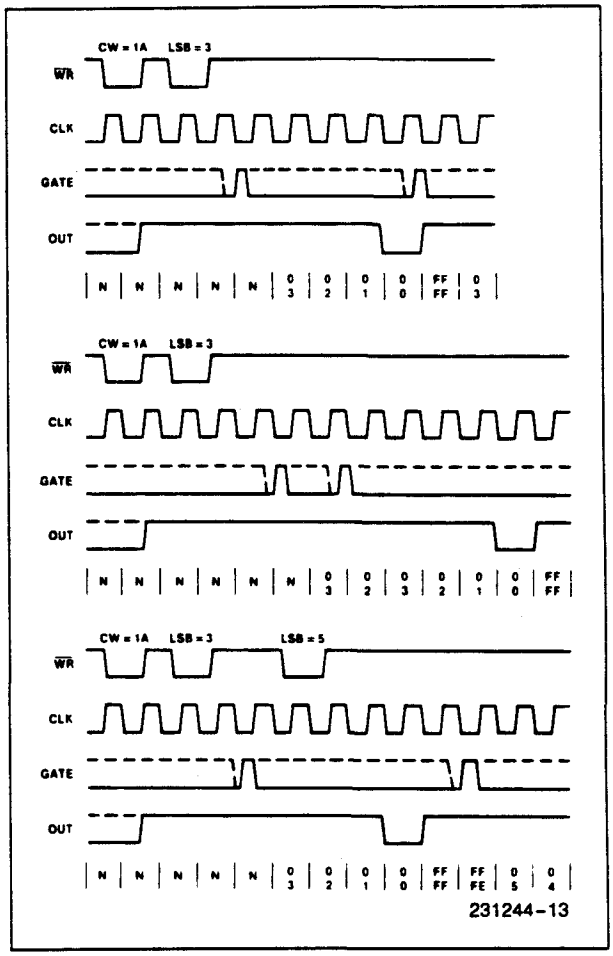


Figure 20. Mode 5

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

Figure 21. Gate Pin Operations Summary

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0

NOTE:
0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting

Figure 22. Minimum and Maximum Initial Counts

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

GATE

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK; the flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs—a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive. In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following $\overline{WR}$ of a new count value.

COUNTER

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

8255 Programmable Peripheral Interface
Data Sheet Reprint

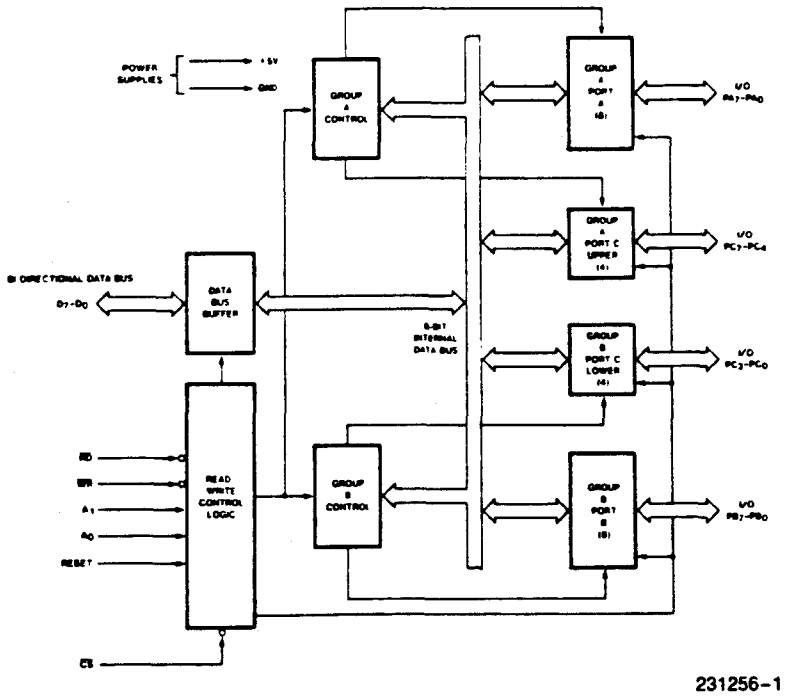
82C55A
CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

- **Compatible with all Intel and Most Other Microprocessors**
- **High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188**
- **24 Programmable I/O Pins**
- **Low Power CHMOS**
- **Completely TTL Compatible**
- **Control Word Read-Back Capability**
- **Direct Bit Set/Reset Capability**
- **2.5 mA DC Drive Capability on all I/O Port Outputs**
- **Available in 40-Pin DIP and 44-Pin PLCC**
- **Available in EXPRESS**
  - **—Standard Temperature Range**
  - **—Extended Temperature Range**

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The 82C55A is pin compatible with the NMOS 8255A and 8255A-5.

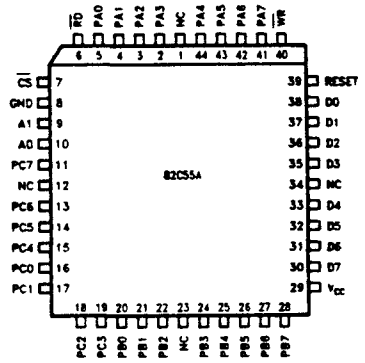
In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

The 82C55A is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.

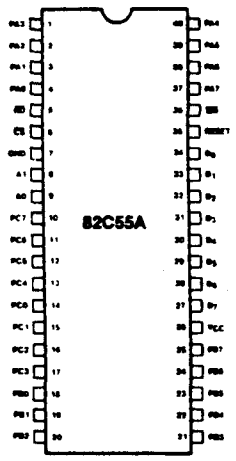


231256-1

Figure 1. 82C55A Block Diagram



231256-31



231256-2

Figure 2. 82C55A Pinout

Diagrams are for pin reference only. Package sizes are not to scale.

September 1987
Order Number: 231256-004

Table 1. Pin Description

Symbol	Pin Number Dip	Pin Number PLCC	Type	Name and Function
PA_{3-0}	1–4	2–5	I/O	**PORT A, PINS 0–3:** Lower nibble of an 8-bit data output latch/ buffer and an 8-bit data input latch.
$\overline{RD}$	5	6	I	**READ CONTROL:** This input is low during CPU read operations.
$\overline{CS}$	6	7	I	**CHIP SELECT:** A low on this input enables the 82C55A to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and WR are ignored otherwise.
GND	7	8		**System Ground**
A_{1-0}	8–9	9–10	I	**ADDRESS:** These input signals, in conjunction $\overline{RD}$ and $\overline{WR}$, control the selection of one of the three ports or the control word registers.
PC_{7-4}	10–13	11,13–15	I/O	**PORT C, PINS 4–7:** Upper nibble of an 8-bit data output latch/ buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
PC_{0-3}	14–17	16–19	I/O	**PORT C, PINS 0–3:** Lower nibble of Port C.
PB_{0-7}	18–25	20–22, 24–28	I/O	**PORT B, PINS 0–7:** An 8-bit data output latch/buffer and an 8-bit data input buffer.
V_{CC}	26	29		**SYSTEM POWER:** + 5V Power Supply.
D_{7-0}	27–34	30–33, 35–38	I/O	**DATA BUS:** Bi-directional, tri-state data bus lines, connected to system data bus.
RESET	35	39	I	**RESET:** A high on this input clears the control register and all ports are set to the input mode.
$\overline{WR}$	36	40	I	**WRITE CONTROL:** This input is low during CPU write operations.
PA_{7-4}	37–40	41–44	I/O	**PORT A, PINS 4–7:** Upper nibble of an 8-bit data output latch/ buffer and an 8-bit data input latch.
NC		1, 12, 23, 34		No Connect

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (Read)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control
					Disable Function
X	X	X	X	1	Data Bus - 3 - State
X	X	1	1	0	Data Bus - 3 - State

82C55A FUNCTIONAL DESCRIPTION

General

The 82C55A is a programmable peripheral interface device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 82C55A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7–C4)
Control Group B - Port B and Port C lower (C3–C0)

The control word register can be both written and read as shown in the address decode table in the pin descriptions. Figure 6 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A. One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both "pull-up" and "pull-down" bus hold devices are present on Port A.

Port B. One 8-bit data input/output latch/buffer. Only "pull-up" bus hold devices are present on Port B.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only "pull-up" bus hold devices are present on Port C.

See Figure 4 for the bus-hold circuit configuration for Port A, B, and C.

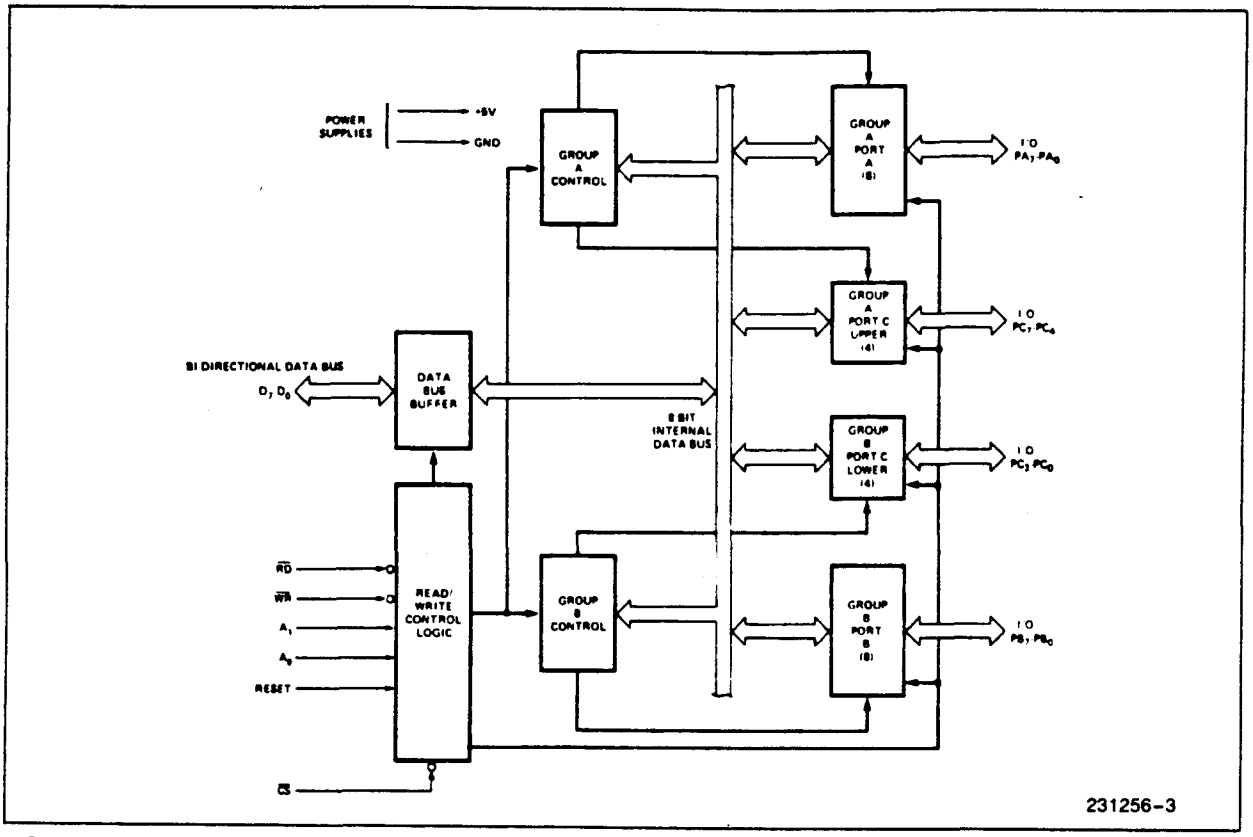
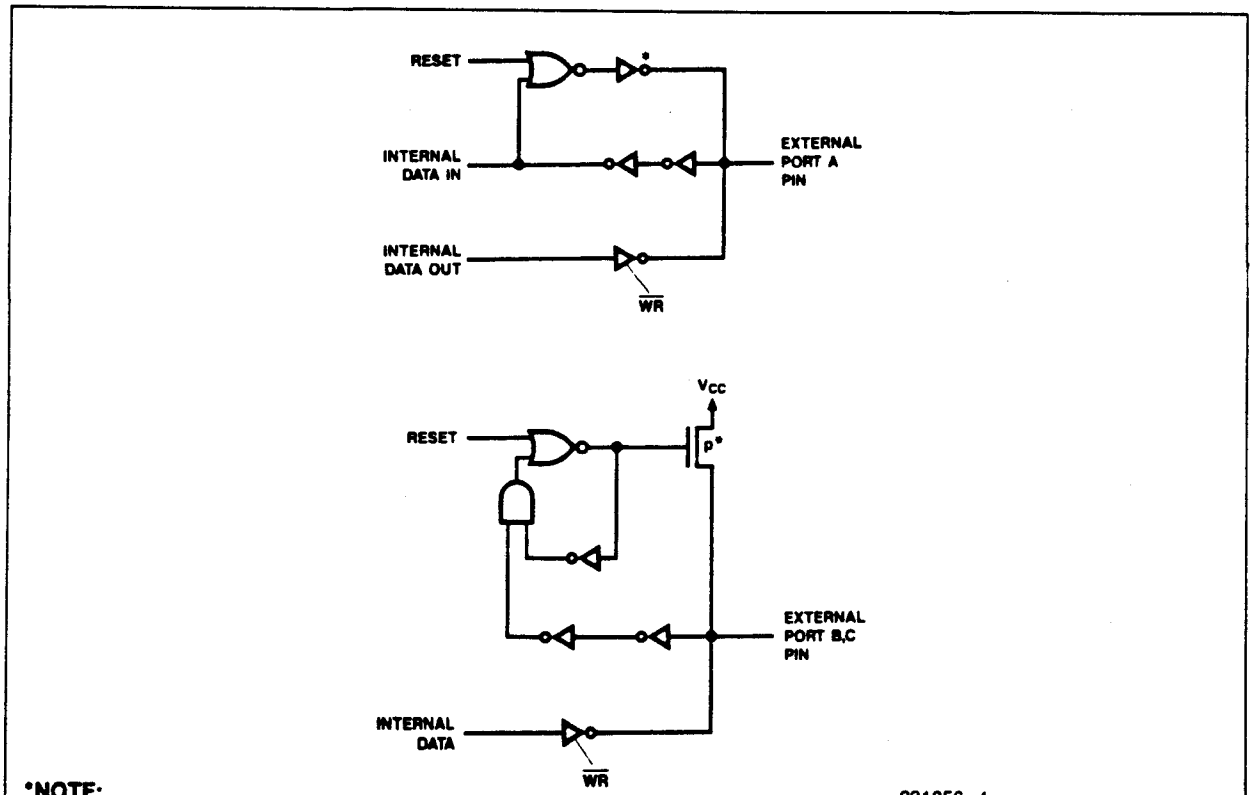


Figure 3. 82C55A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions



*NOTE:
Port pins loaded with more than 20 pF capacitance may not have their logic level guaranteed following a hardware reset.

Figure 4. Port A, B, C, Bus-hold Configuration

82C55A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 — Basic input/output
Mode 1 — Strobed Input/output
Mode 2 — Bi-directional Bus

When the reset input goes "high" all ports will be set to the input mode with all 24 port lines held at a logic "one" level by the internal bus hold devices (see Figure 4 Note). After the reset is removed the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown devices in "all CMOS" designs. During the execution of the system program, any of the other modes may be selected by using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

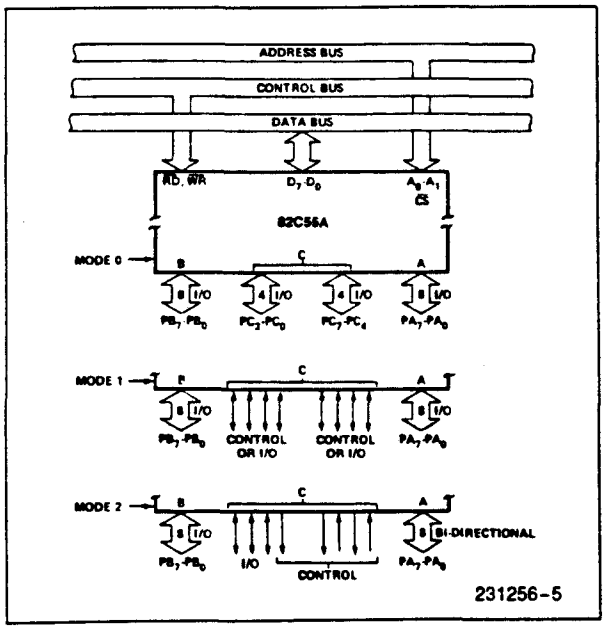


Figure 5. Basic Mode Definitions and Bus Interface

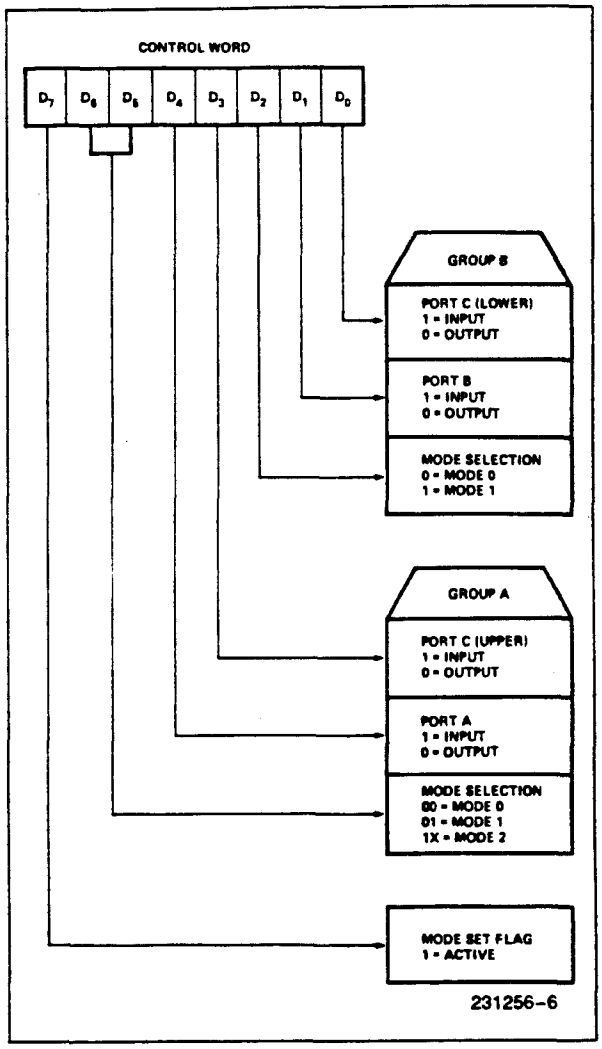


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

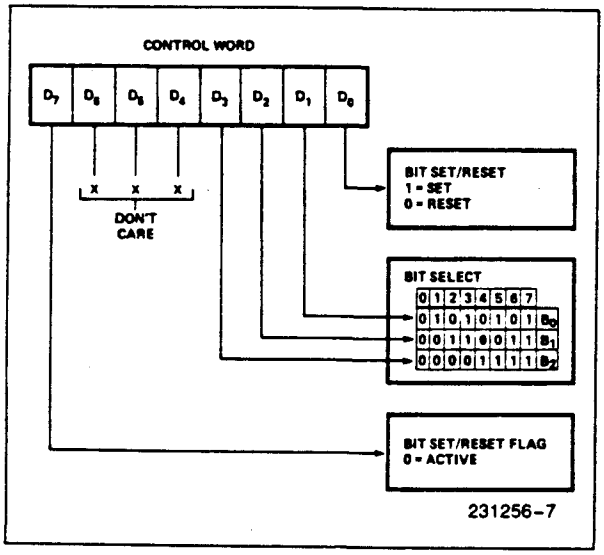

CONTROL WORD
D7 D6 D5 D4 D3 D2 D1 D0
X X X
DON'T CARE
BIT SET/RESET
1 = SET
0 = RESET
BIT SELECT
0 1 2 3 4 5 6 7
0 1 0 1 0 1 0 1 B0
0 0 1 1 0 0 1 1 B1
0 0 0 0 1 1 1 1 B2
BIT SET/RESET FLAG
0 = ACTIVE
231256-7

Figure 7. Bit Set/Reset Format

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is SET—Interrupt enable
(BIT-RESET)—INTE is RESET—Interrupt disable

Note:
All Mask flip-flops are automatically reset during mode selection and device Reset.

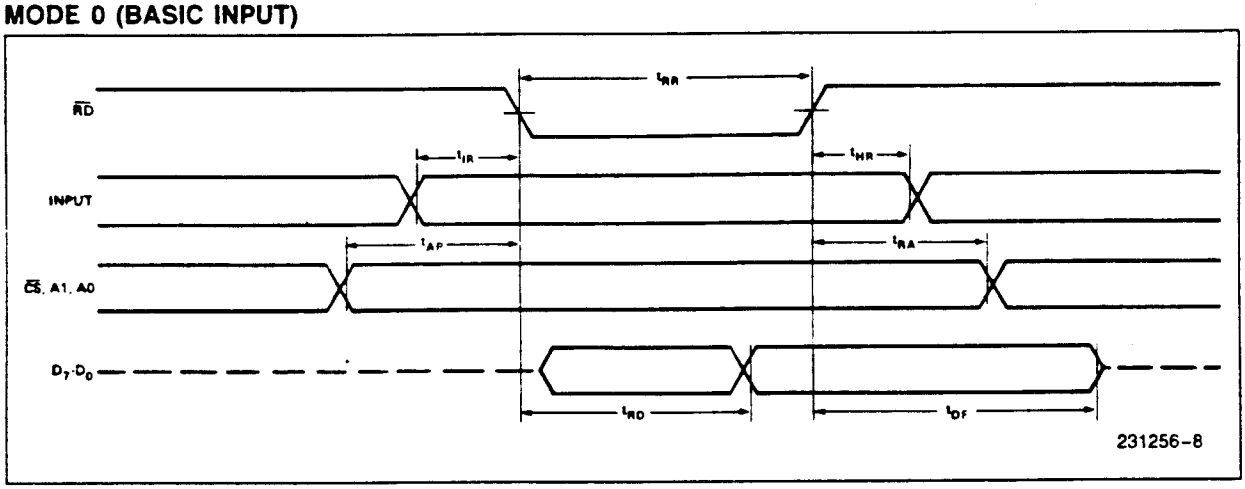
Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

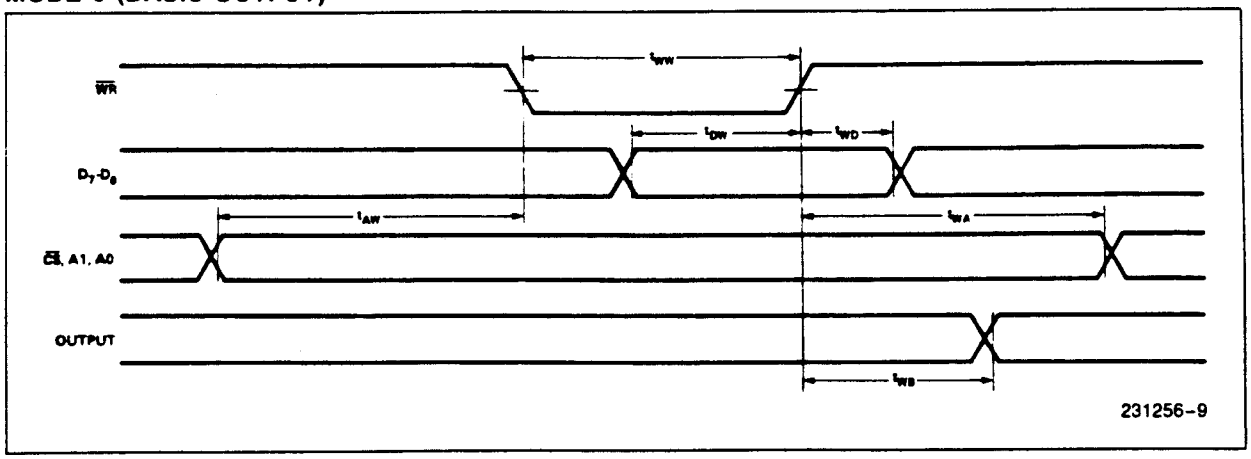
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

MODE 0 (BASIC INPUT)



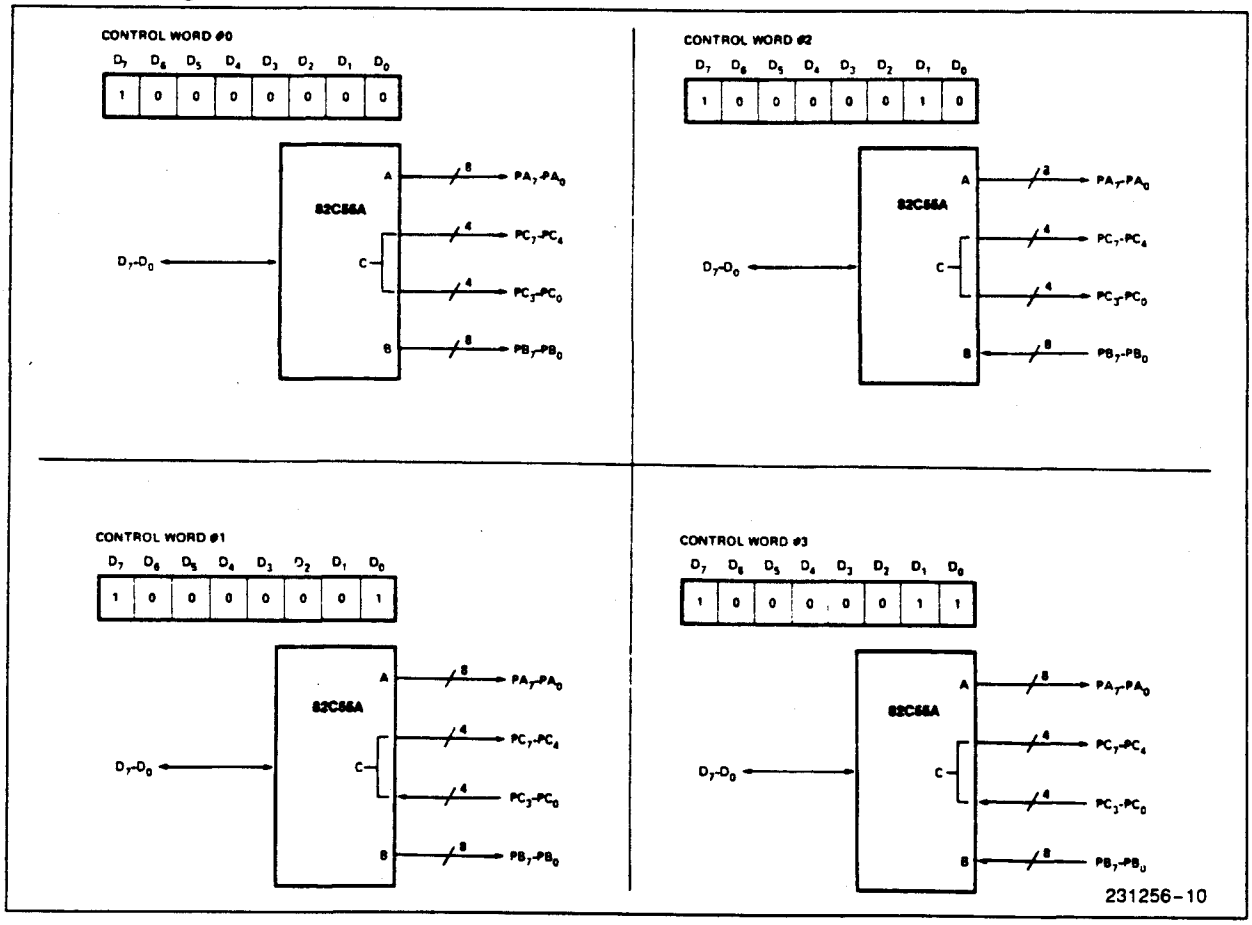
MODE 0 (BASIC OUTPUT)



MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

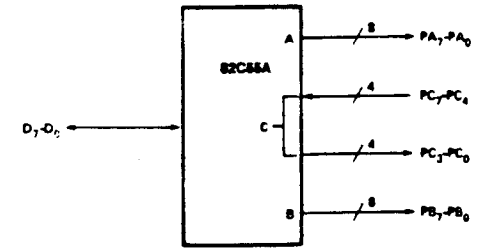
MODE 0 Configurations



MODE 0 Configurations (Continued)

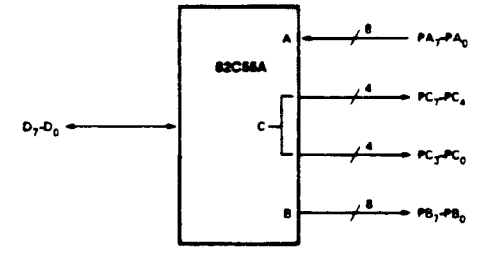
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



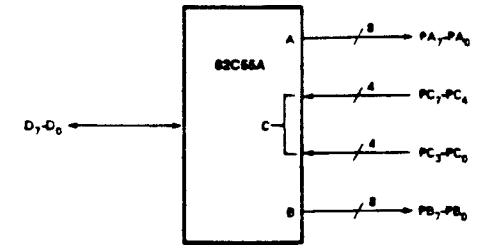
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



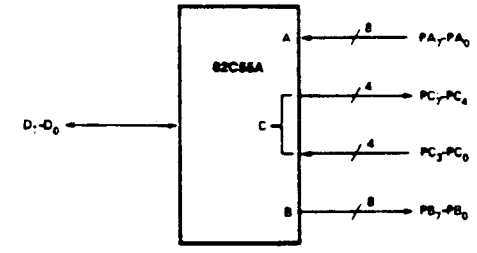
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



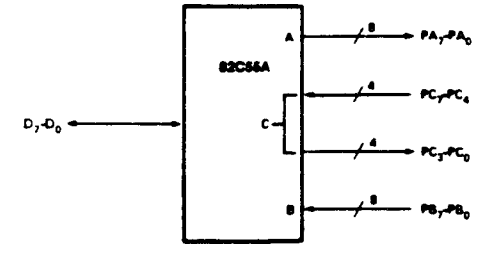
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



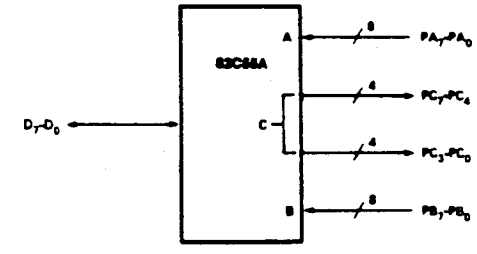
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



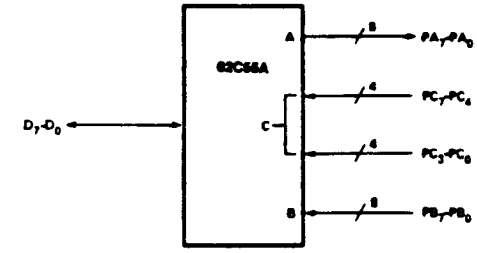
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



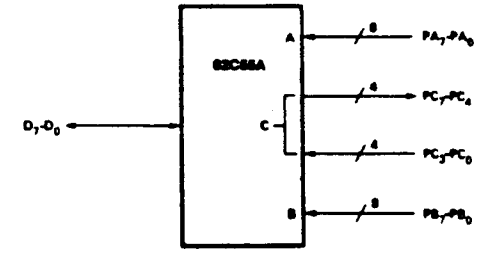
CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1



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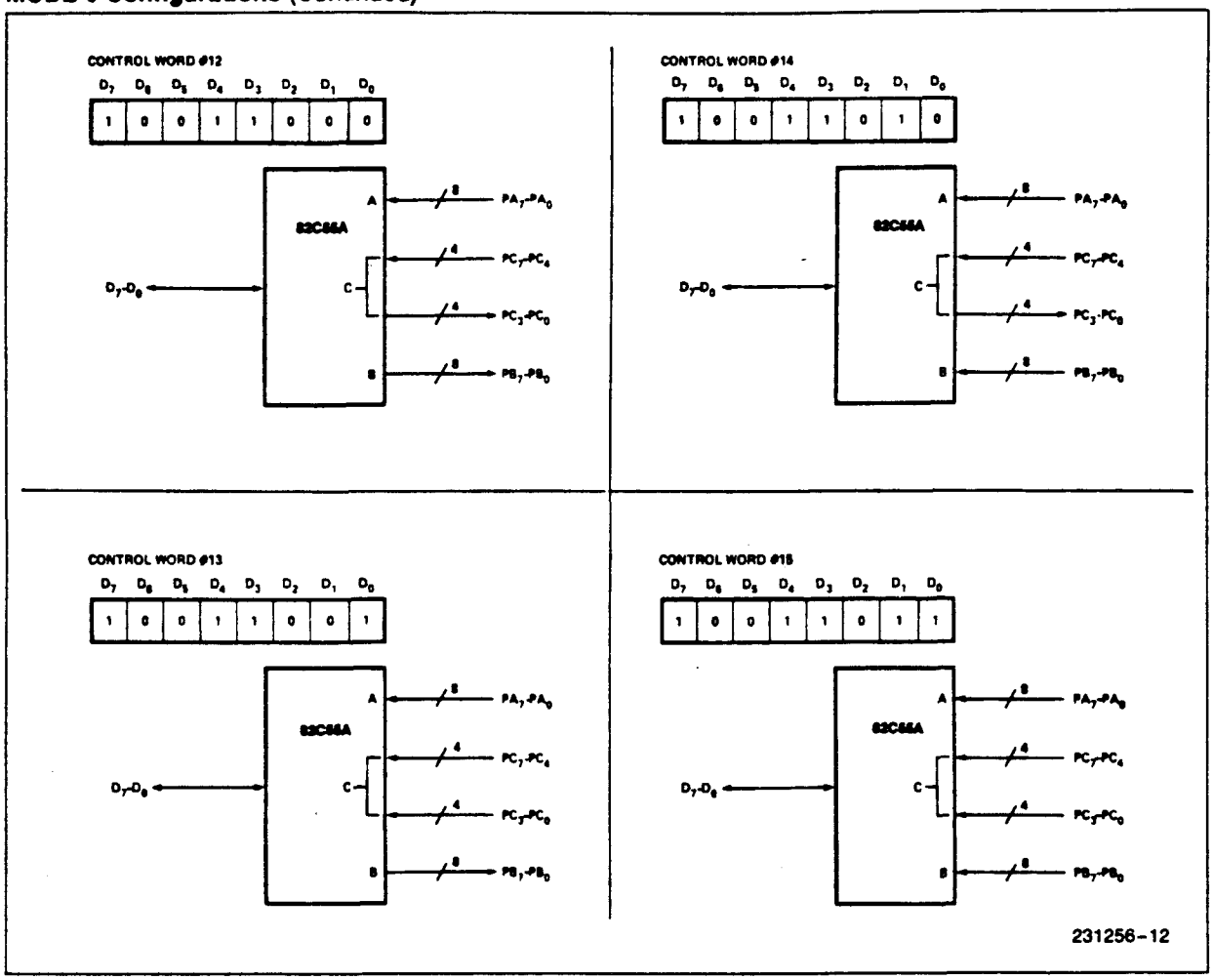
MODE 0 Configurations (Continued)



Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

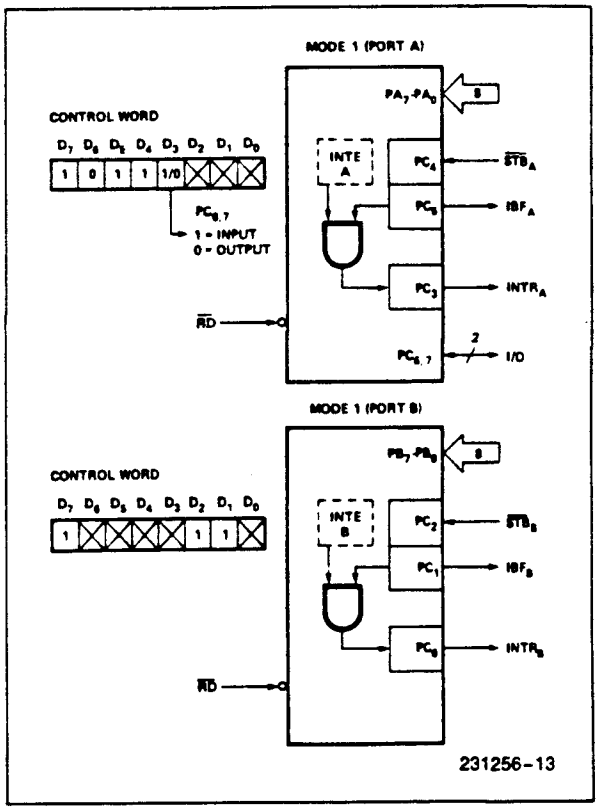


Figure 8. MODE 1 Input

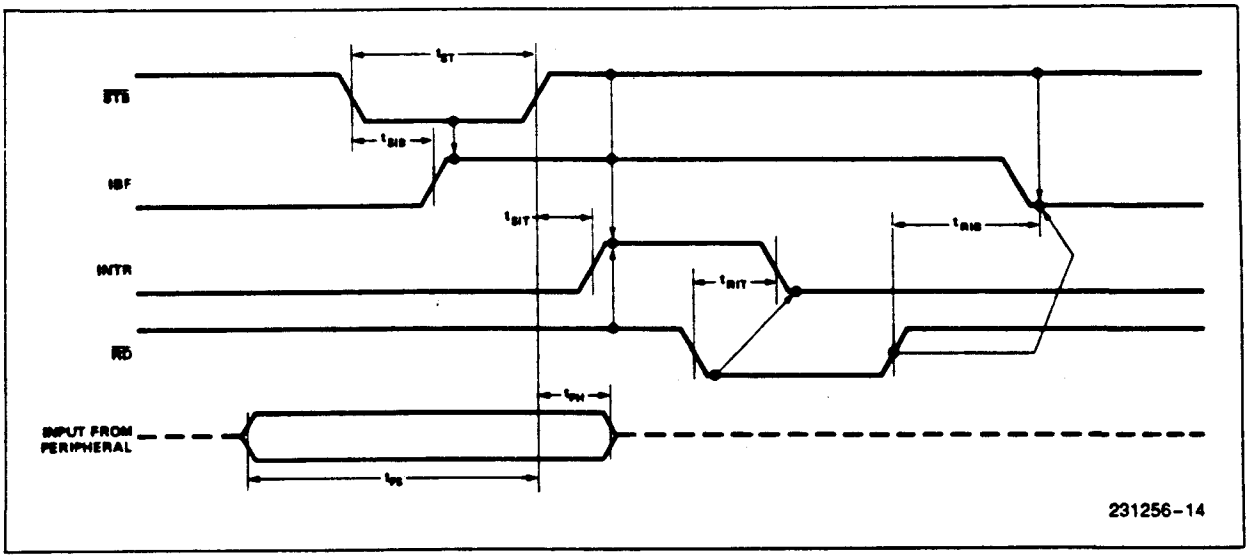


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ Input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 82C55A that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

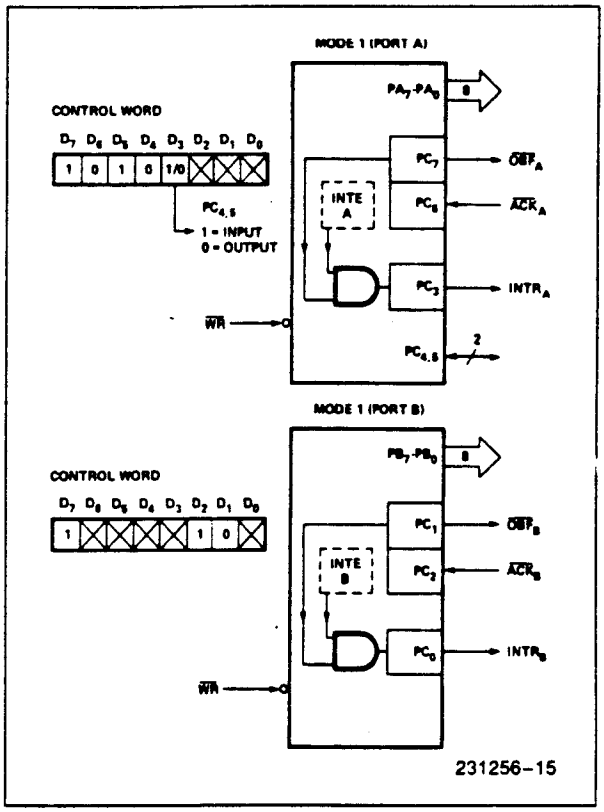


Figure 10. MODE 1 Output

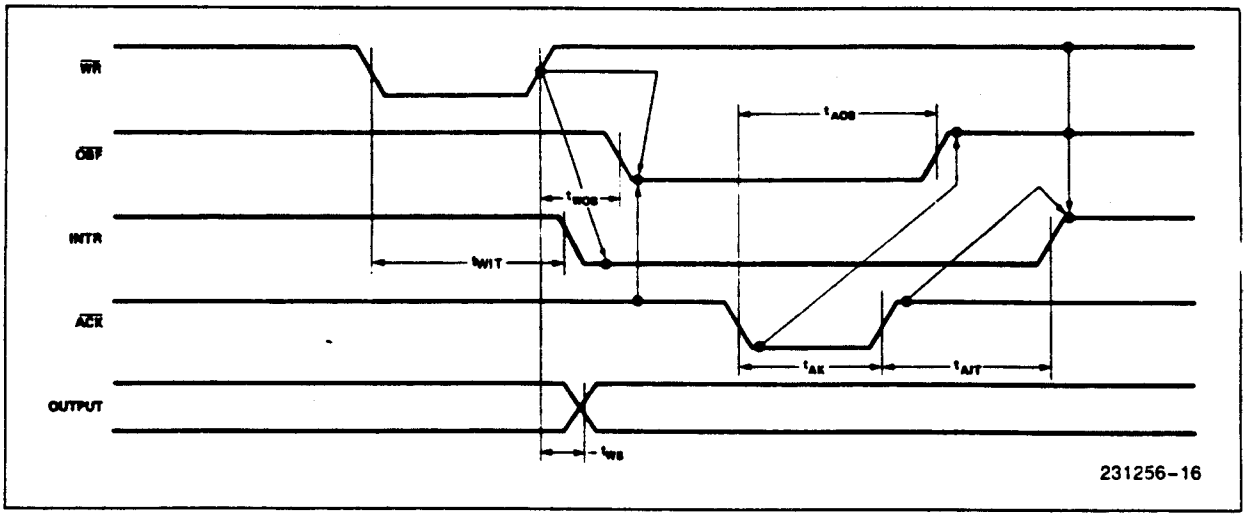


Figure 11. MODE 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

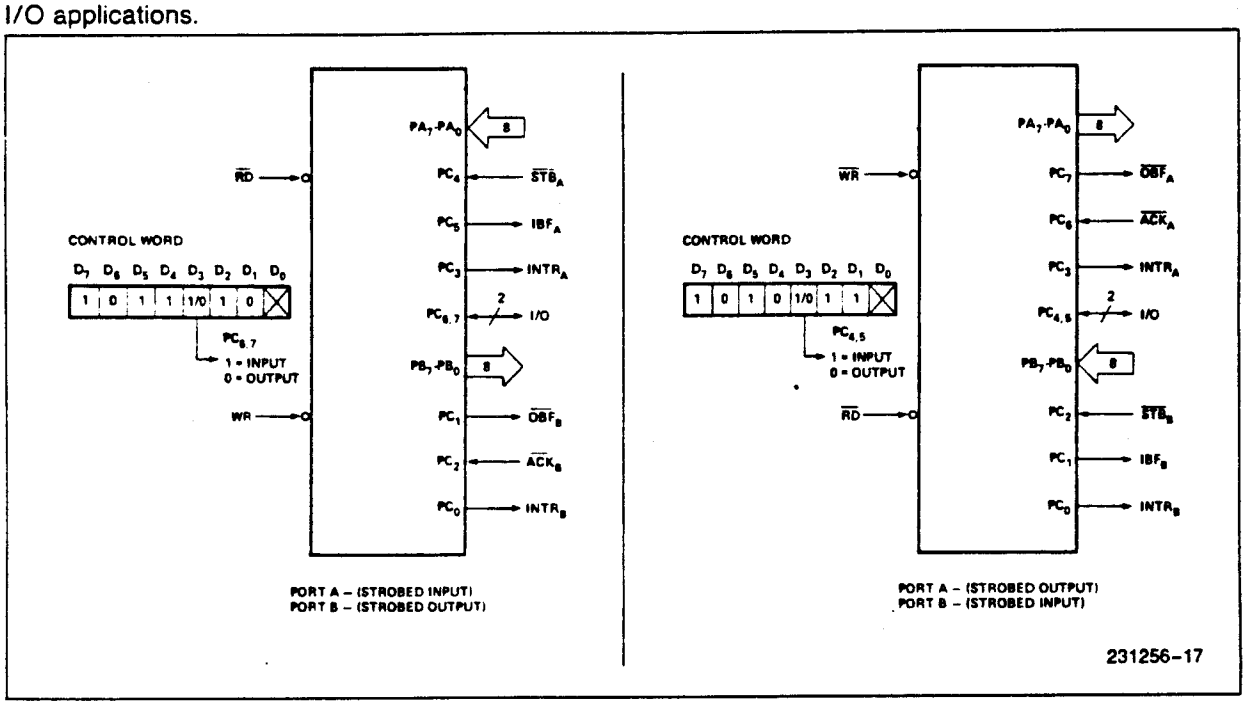


Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A **only**.
- One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

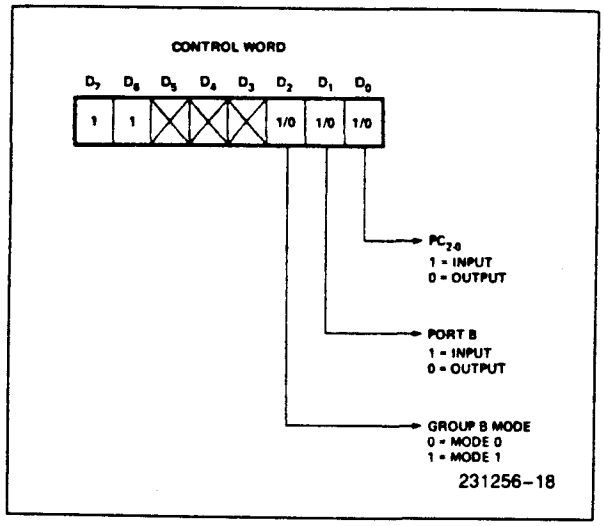


Figure 13. MODE Control Word

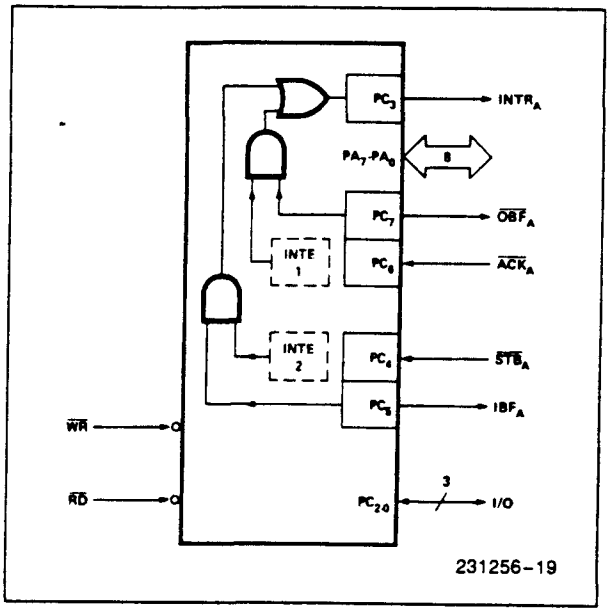


Figure 14. MODE 2

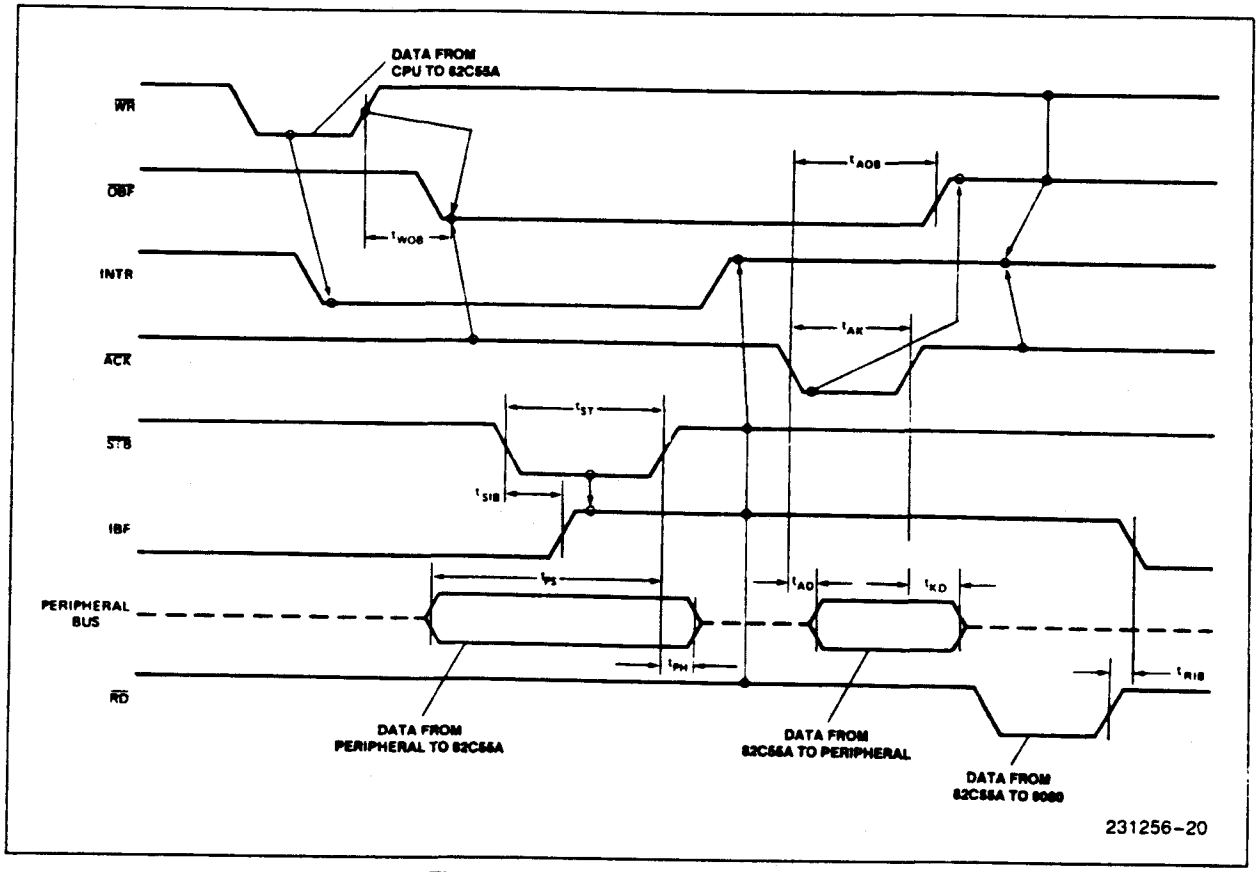


Figure 15. MODE 2 (Bidirectional)

NOTE:
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$, and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

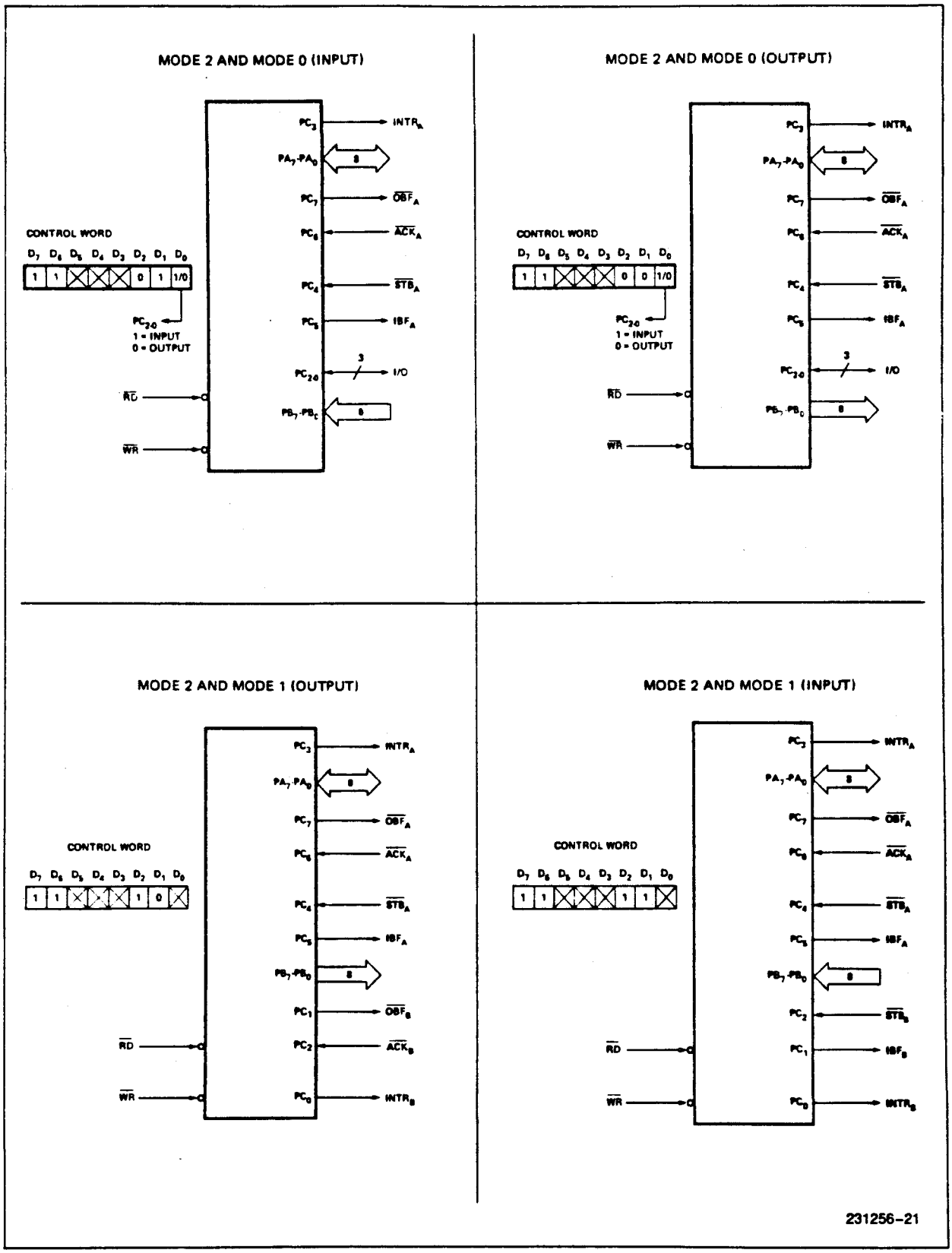


Figure 16. MODE 1/4 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	↔	
PA_1	IN	OUT	IN	OUT	↔	
PA_2	IN	OUT	IN	OUT	↔	
PA_3	IN	OUT	IN	OUT	↔	
PA_4	IN	OUT	IN	OUT	↔	
PA_5	IN	OUT	IN	OUT	↔	
PA_6	IN	OUT	IN	OUT	↔	
PA_7	IN	OUT	IN	OUT	↔	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 18.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 18.

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5 mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

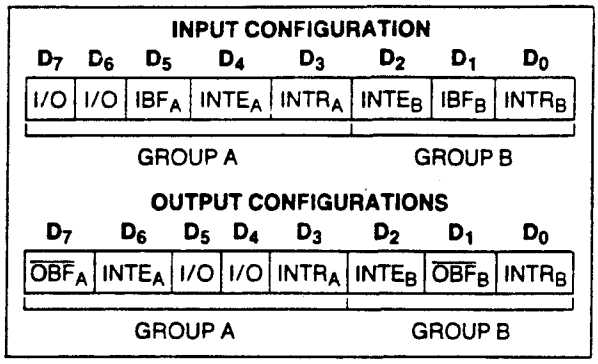

INPUT CONFIGURATION
D7 D6 D5 D4 D3 D2 D1 D0
I/O I/O IBFA INTEA INTRA INTEB IBFB INTRB
GROUP A
GROUP B
OUTPUT CONFIGURATIONS
D7 D6 D5 D4 D3 D2 D1 D0
OBFA INTEA I/O I/O INTRA INTEB OBFB INTRB
GROUP A
GROUP B

Figure 17a. MODE 1 Status Word Format

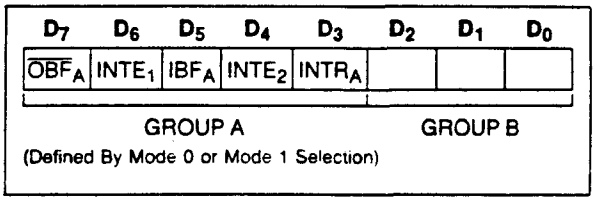


Figure 17b. MODE 2 Status Word Format

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
INTE B	PC2	$\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1)
INTE A2	PC4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2

Figure 18. Interrupt Enable Flags in Modes 1 and 2

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias....0°C to + 70°C
Storage Temperature .....− 65°C to + 150°C
Supply Voltage .....− 0.5 to + 8.0V
Operating Voltage .....+ 4V to + 7V
Voltage on any Input.....GND−2V to + 6.5V
Voltage on any Output ..GND−0.5V to V_{CC} + 0.5V
Power Dissipation .....1 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, GND = 0V (T_A = −40°C to +85°C for Extended Temperture)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output High Voltage	3.0 V_{CC} − 0.4		V V	I_{OH} = −2.5 mA I_{OH} = −100 μA
I_{IL}	Input Leakage Current		±1	μA	V_{IN} = V_{CC} to 0V (Note 1)
I_{OFL}	Output Float Leakage Current		±10	μA	V_{IN} = V_{CC} to 0V (Note 2)
I_{DAR}	Darlington Drive Current	±2.5	(Note 4)	mA	Ports A, B, C R_{ext} = 500Ω V_{ext} = 1.7V
I_{PHL}	Port Hold Low Leakage Current	+50	+300	μA	V_{OUT} = 1.0V Port A only
I_{PHH}	Port Hold High Leakage Current	−50	−300	μA	V_{OUT} = 3.0V Ports A, B, C
I_{PHLO}	Port Hold Low Overdrive Current	−350		μA	V_{OUT} = 0.8V
I_{PHHO}	Port Hold High Overdrive Current	+350		μA	V_{OUT} = 3.0V
I_{CC}	V_{CC} Supply Current		10	mA	(Note 3)
I_{CCSB}	V_{CC} Supply Current-Standby		10	μA	V_{CC} = 5.5V V_{IN} = V_{CC} or GND Port Conditions If I/P = Open/High O/P = Open Only With Data Bus = High/Low $\overline{CS}$ = High Reset = Low Pure Inputs = Low/High

NOTES:
1. Pins A_1, A_0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Reset.
2. Data Bus; Ports B, C.
3. Outputs open.
4. Limit output current to 4.0 mA.

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance		10	pF	Unmeasured pins returned to GND f_c = 1 MHz(5)
$C_{I/O}$	I/O Capacitance		20	pF	

NOTE:
5. Sampled not 100% tested.

A.C. CHARACTERISTICS

T_A = 0° to 70°C, V_{CC} = +5V ±10%, GND = 0V

T_A = −40°C to +85°C for Extended Temperature

BUS PARAMETERS

READ CYCLE

Symbol	Parameter	82C55A-2		Units	Test Conditions
		Min	Max		
t_{AR}	Address Stable Before $\overline{RD}\downarrow$	0		ns	
t_{RA}	Address Hold Time After $\overline{RD}\uparrow$	0		ns	
t_{RR}	$\overline{RD}$ Pulse Width	150		ns	
t_{RD}	Data Delay from $\overline{RD}\downarrow$		120	ns	
t_{DF}	$\overline{RD}\uparrow$ to Data Floating	10	75	ns	
t_{RV}	Recovery Time between $\overline{RD}/\overline{WR}$	200		ns	

WRITE CYCLE

Symbol	Parameter	82C55A-2		Units	Test Conditions
		Min	Max		
t_{AW}	Address Stable Before $\overline{WR}\downarrow$	0		ns	
t_{WA}	Address Hold Time After $\overline{WR}\uparrow$	20		ns	Ports A & B
		20		ns	Port C
t_{WW}	$\overline{WR}$ Pulse Width	100		ns	
t_{DW}	Data Setup Time Before $\overline{WR}\uparrow$	100		ns	
t_{WD}	Data Hold Time After $\overline{WR}\uparrow$	30		ns	Ports A & B
		30		ns	Port C

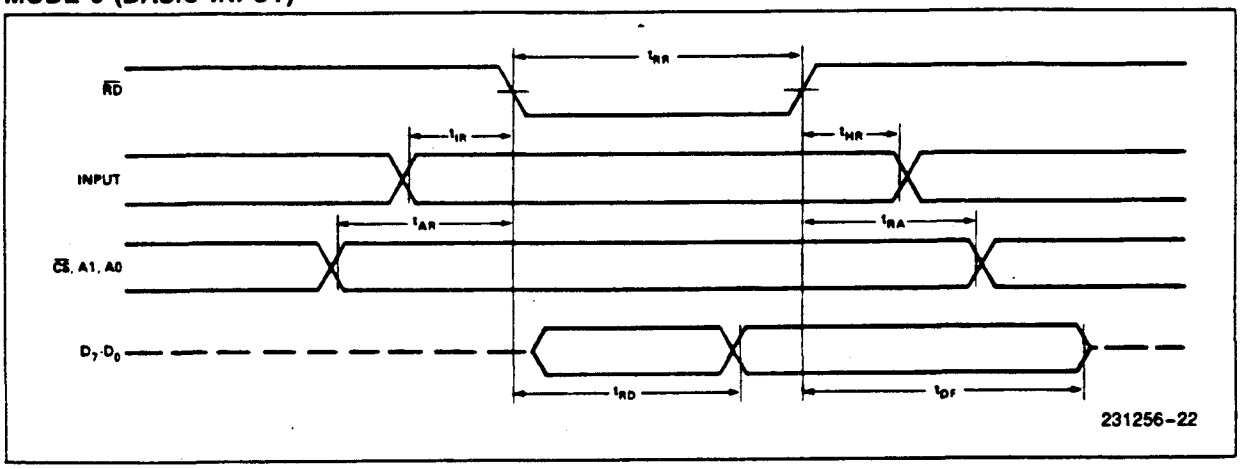
OTHER TIMINGS

Symbol	Parameter	82C55A-2		Units Conditions	Test
		Min	Max		
t_{WB}	$\overline{WR}$ = 1 to Output		350	ns	
t_{IR}	Peripheral Data Before $\overline{RD}$	0		ns	
t_{HR}	Peripheral Data After $\overline{RD}$	0		ns	
t_{AK}	$\overline{ACK}$ Pulse Width	200		ns	
t_{ST}	$\overline{STB}$ Pulse Width	100		ns	
t_{PS}	Per. Data Before $\overline{STB}$ High	20		ns	
t_{PH}	Per. Data After $\overline{STB}$High	50		ns	
t_{AD}	$\overline{ACK}$ = 0 to Output		175	ns	
t_{KD}	$\overline{ACK}$ = 1 to Output Float	20	250	ns	
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = O		150	ns	
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1		150	ns	
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1		150	ns	
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0		150	ns	
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0		200	ns	
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1		150	ns	
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1		150	ns	
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0		200	ns	see note 1
t_{RES}	Reset Pulse Width	500		ns	see note 2

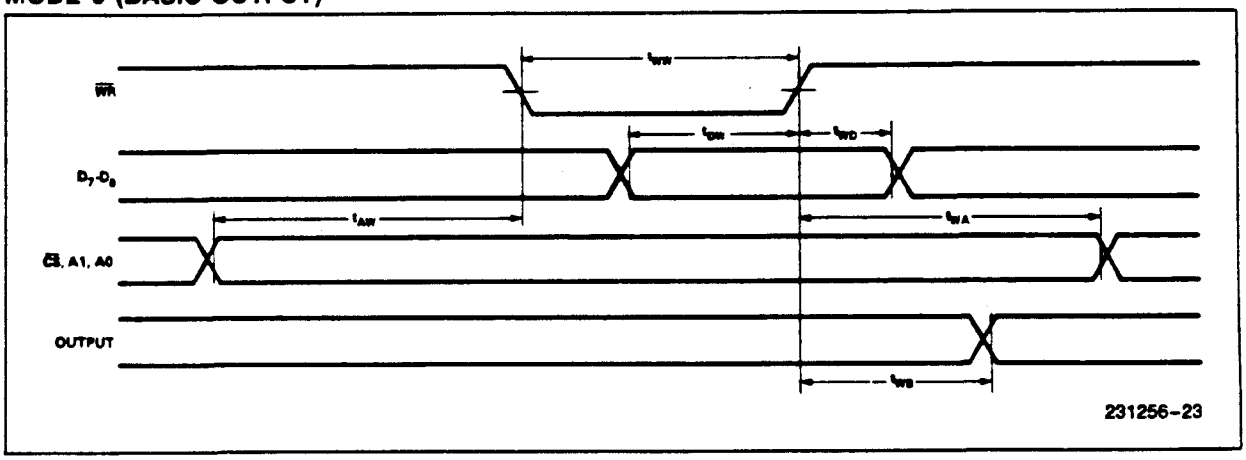
NOTE:
1. INTR ↑ may occur as early as $\overline{WR}$ ↓.
2. Pulse width of initial Reset pulse after power on must be at least 50 μSec. Subsequent Reset pulses may be 500 ns minimum.

WAVEFORMS

MODE 0 (BASIC INPUT)

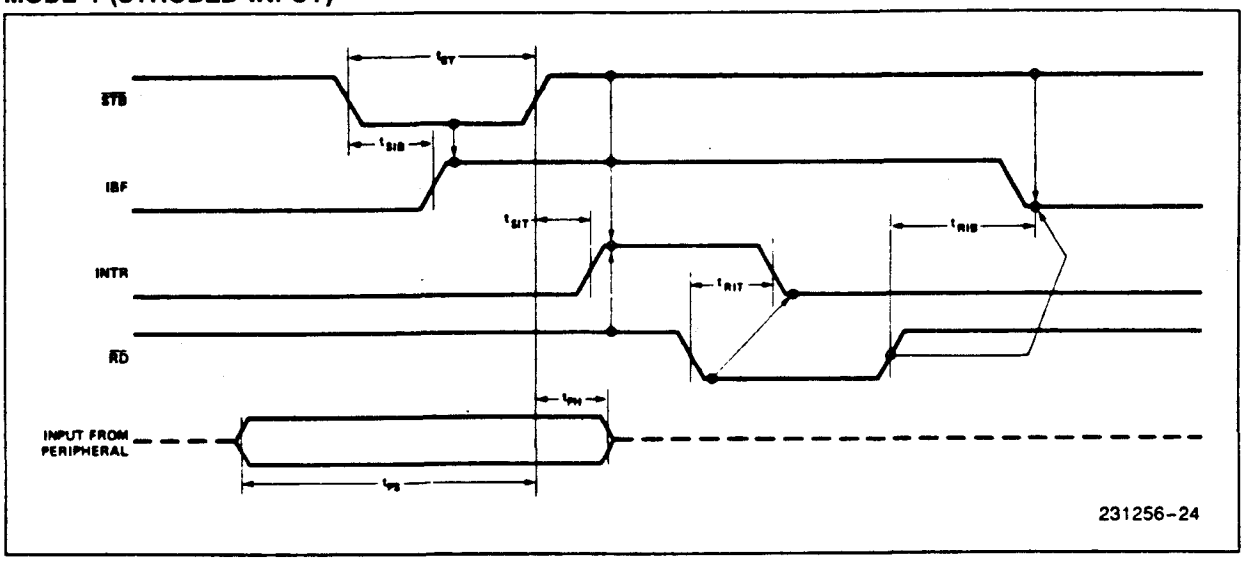


MODE 0 (BASIC OUTPUT)

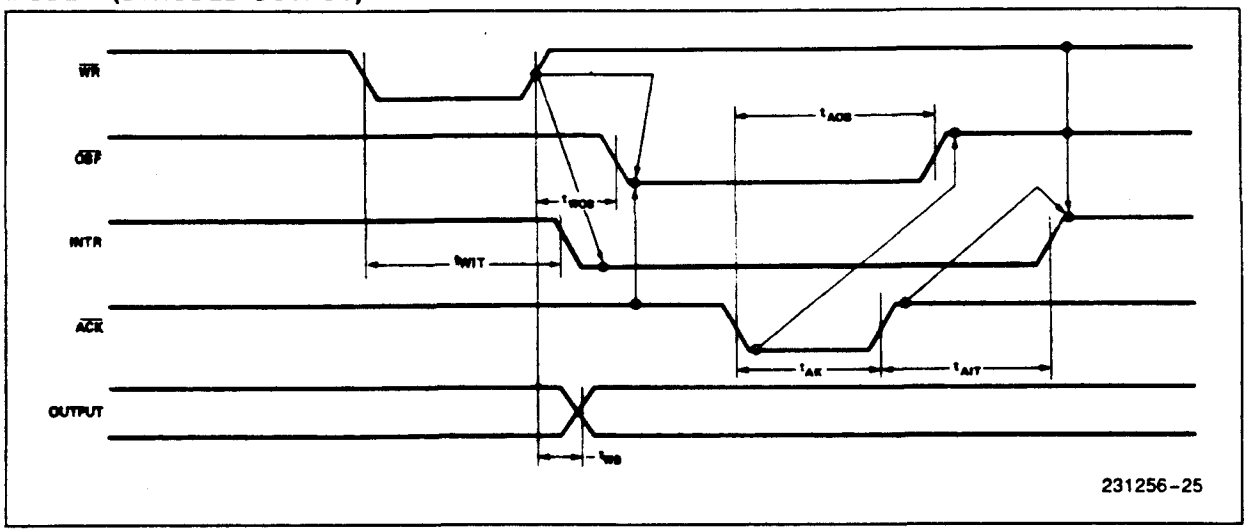


WAVEFORMS (Continued)

MODE 1 (STROBED INPUT)

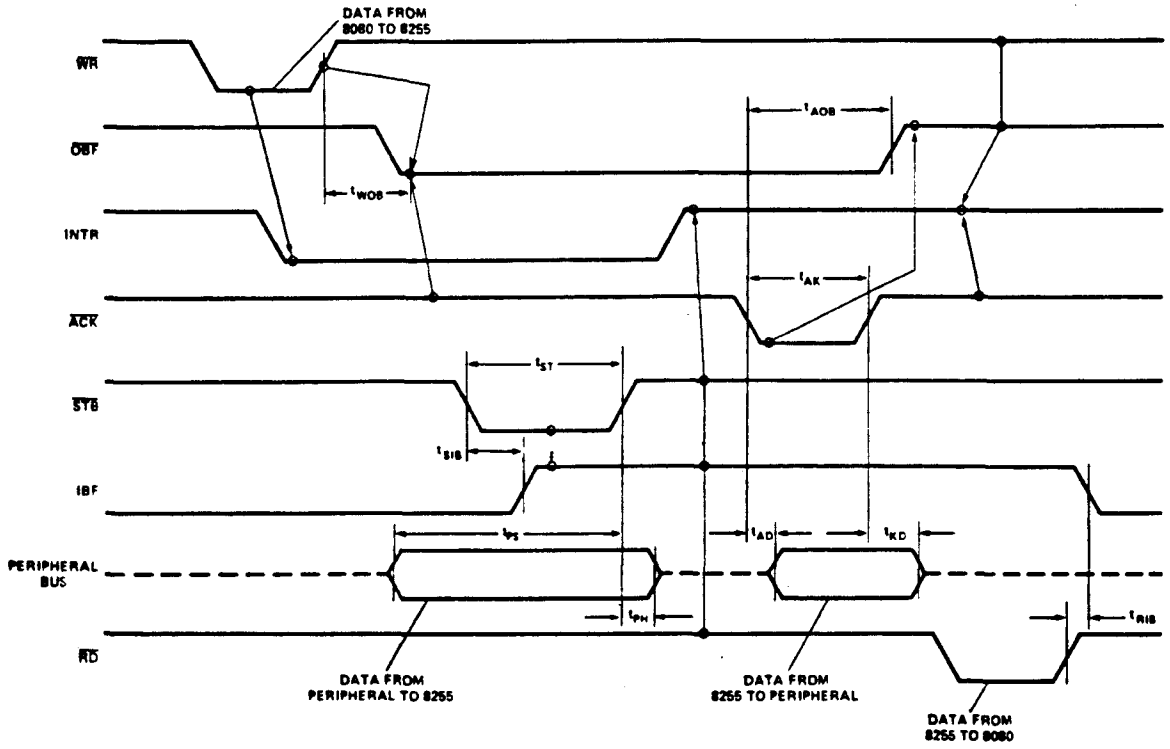


MODE 1 (STROBED OUTPUT)



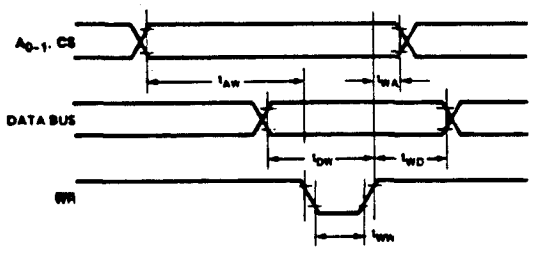
WAVEFORMS (Continued)

MODE 2 (BIDIRECTIONAL)

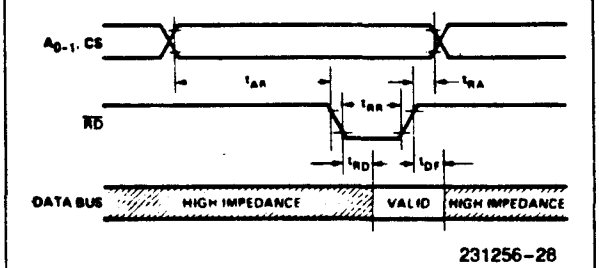


Note:
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ AND $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \bullet \overline{MASK} \bullet \overline{STB} \bullet \overline{RD} + \overline{OBF} \bullet \overline{MASK} \bullet \overline{ACK} \bullet \overline{WR}$)

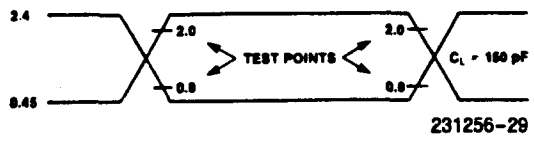
WRITE TIMING



READ TIMING

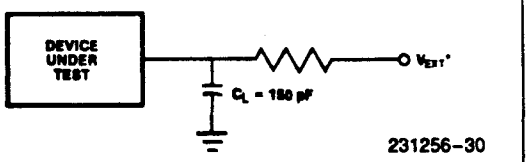


A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing Inputs Are Driven At 2.4V For A Logic 1 And 0.45V For A Logic 0 Timing Measurements Are Made At 2.0V For A Logic 1 And 0.8 For A Logic 0.

A.C. TESTING LOAD CIRCUIT



*V_{EXT} Is Set At Various Voltages During Testing To Guarantee The Specification. C_L Includes Jig Capacitance.

APPENDIX D

WARRANTY

LIMITED WARRANTY

Real Time Devices, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from REAL TIME DEVICES. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, REAL TIME DEVICES will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to REAL TIME DEVICES. All replaced parts and products become the property of REAL TIME DEVICES. **Before returning any product for repair, customers are required to contact the factory for an RMA number.**

THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY PRODUCTS WHICH HAVE BEEN DAMAGED AS A RESULT OF ACCIDENT, MISUSE, ABUSE (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by REAL TIME DEVICES, "acts of God" or other contingencies beyond the control of REAL TIME DEVICES), OR AS A RESULT OF SERVICE OR MODIFICATION BY ANYONE OTHER THAN REAL TIME DEVICES. EXCEPT AS EXPRESSLY SET FORTH ABOVE, NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND REAL TIME DEVICES EXPRESSLY DISCLAIMS ALL WARRANTIES NOT STATED HEREIN. ALL IMPLIED WARRANTIES, INCLUDING IMPLIED WARRANTIES FOR MECHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED TO THE DURATION OF THIS WARRANTY. IN THE EVENT THE PRODUCT IS NOT FREE FROM DEFECTS AS WARRANTED ABOVE, THE PURCHASER'S SOLE REMEDY SHALL BE REPAIR OR REPLACEMENT AS PROVIDED ABOVE. UNDER NO CIRCUMSTANCES WILL REAL TIME DEVICES BE LIABLE TO THE PURCHASER OR ANY USER FOR ANY DAMAGES, INCLUDING ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES, EXPENSES, LOST PROFITS, LOST SAVINGS, OR OTHER DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE THE PRODUCT.

SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES FOR CONSUMER PRODUCTS, AND SOME STATES DO NOT ALLOW LIMITATIONS ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATIONS OR EXCLUSIONS MAY NOT APPLY TO YOU.

THIS WARRANTY GIVES YOU SPECIFIC LEGAL RIGHTS, AND YOU MAY ALSO HAVE OTHER RIGHTS WHICH VARY FROM STATE TO STATE.

VF910 Board User-Selected Settings	
Base I/O Address:	
(hex)	(decimal)